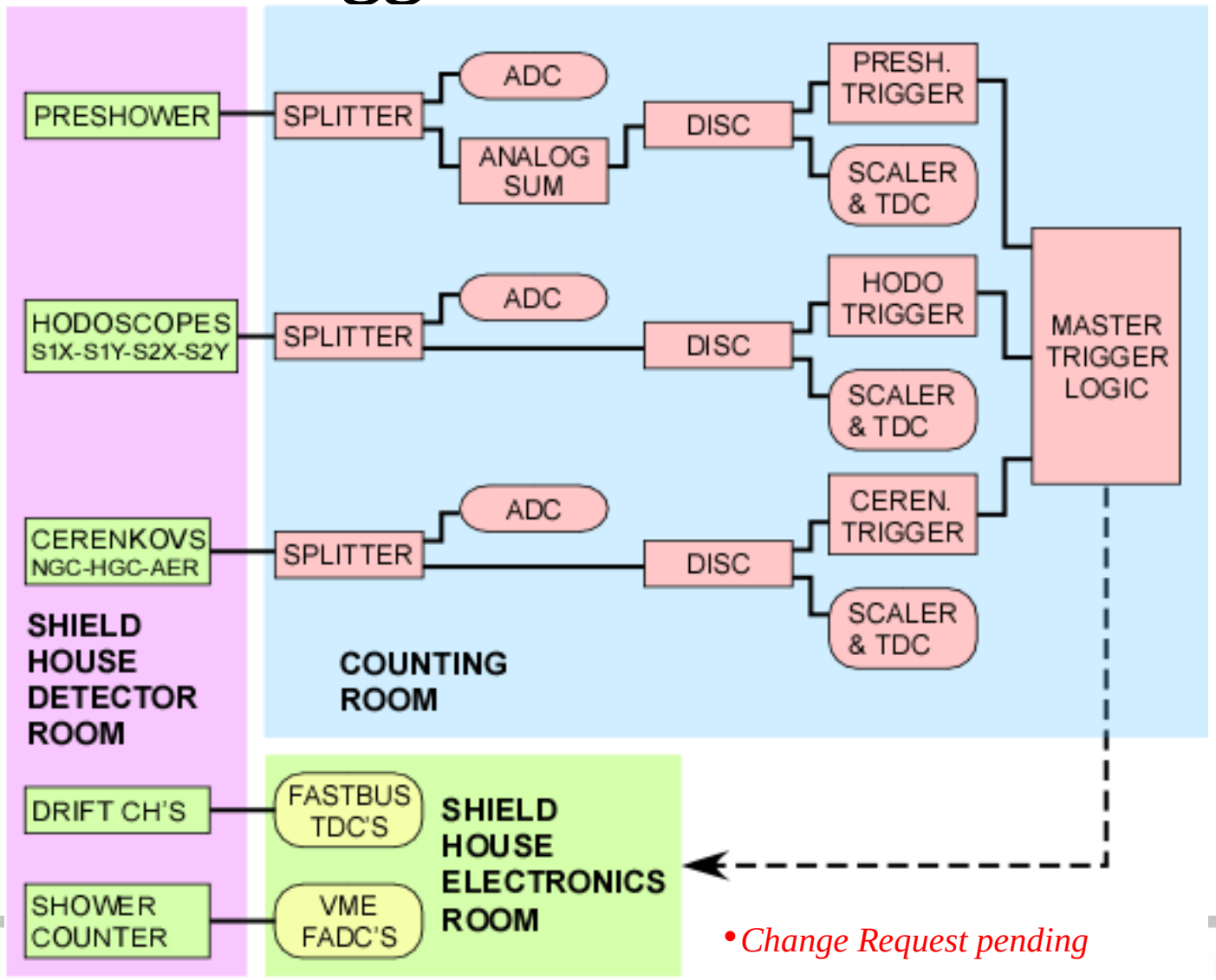
PR12-11-009 GeN
DAQ / Software Options

Brad Sawatzky (JLab/Hall C)

SHMS Readout Plans

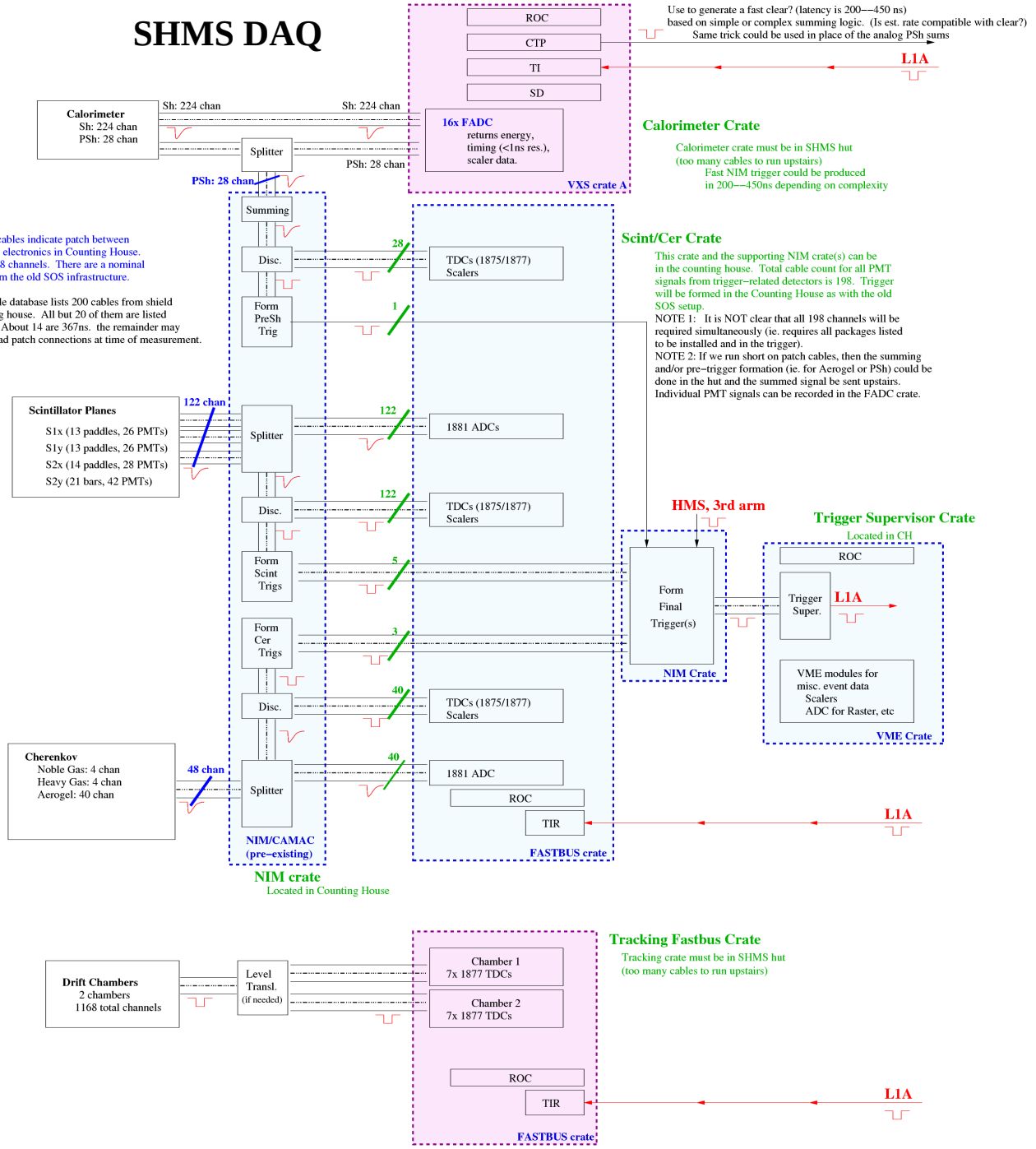
12 GeV* Base Project SHMS Trigger/Electronics

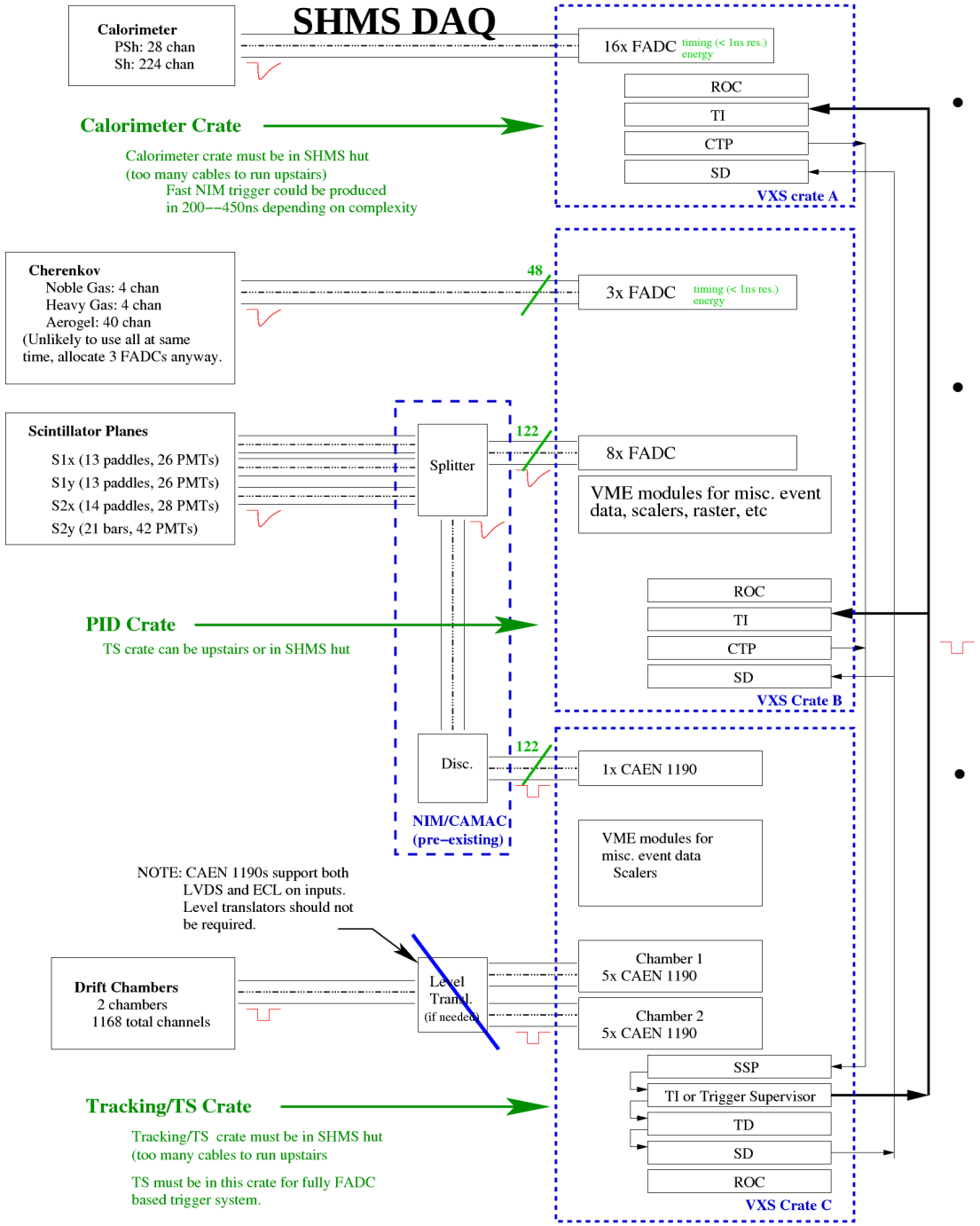


• *Change Request pending*

Hybrid/Legacy Trigger

- Basically the same as the HMS system, but with FADCs reading out Calorimeter
  - This is our 12 GeV starting point.
- FADCs can provide ADC, TDC (~1 ns res.), and scaler data
- If desired, Calo. FADCs could provide a simple sum, or more sophisticated cluster trigger with latency of ~200—400ns
  - too slow to be in main trigger, but could be used as a fast clear
- If all 3 Cherenkov's in use (40+4+4 ch), we require 198/200 existing SOS patch cables... pretty tight fit.
  - Could sum in SHMS hut for trigger if needed.
- FASTBUS electronics will be replaced with FADCs (running in 'legacy' integrating mode) and VME TDCs as early as is practical.
  - The legacy NIM trigger will be maintained.





Modern Trigger/DAQ

- "Stage 2" evolution of system
  - fully pipelined capable
  - 'deadtimeless' operation at >10kHz possible
- Legacy/NIM logic will be left in place and can be used as either primary or auxilliary trigger.
  - (Will need legacy trigger to debug/cross-check any FADC logic anyway)
- DAQ can be configured for:
  - high-speed fully-pipelined mode
    - trigger can be generated in NIM logic, *or* in firmware
  - "Hybrid mode"
    - ie. in conjunction with non -pipelined 3rd arm, etc.

NPOL Readout Options

Basic Assumptions

- 218 scintillator bars
  - 80 E counters (top + bottom)
  - 78 dE vetos (top + bottom)
  - 12 forward vetos
    - very high rates, need good timing & short pulse widths
  - 48 analyzer bars
    - very high rates in forward analyzers
- All bars double-ended readout
  - 436 PMTs
  - Timing: R+L coincidence on every bar for
    - BG suppression
    - position information (what is minimum hardware timing resolution?)
  - Energy/ADC:
    - dE/E on upper/lower bars,
    - walk-correction on TDC timing
- NPOL readout electronics likely located in the Hall
  - not enough patch cables to run upstairs

Trigger Options

- Read out everything for all SHMS triggers?
  - Proposal suggests max SHMS trigger rate < 1kHz (?)
  - Data rate and storage requirements are small by present standards
  - SHMS DAQ will be able to handle 2—3 kHz readout rates with no effort
    - 4—5 kHz is achievable with a little work, even with legacy electronics on the NPOL side; it would be no problem with modern readout electronics
- Will want NPOL singles trigger too, but life is a little simpler if we do not require hardware NPOL+SHMS coincidence trigger
- Trigger-level NPOL+SHMS coin. is manageable too, of course
  - have a couple options here (conventional, pipelined)

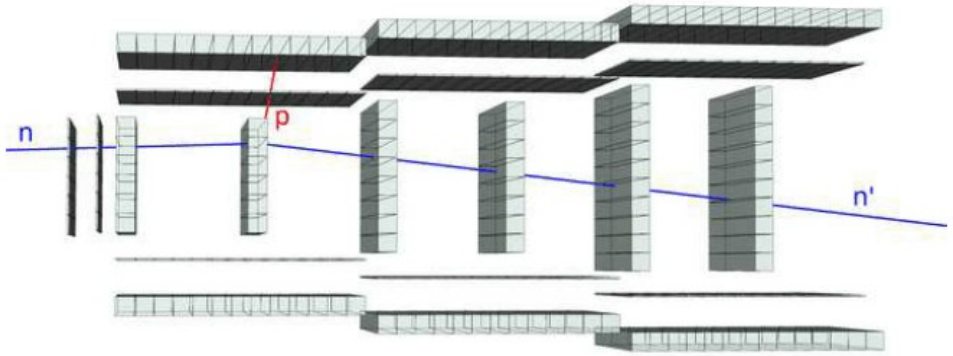
Readout Options: TDC

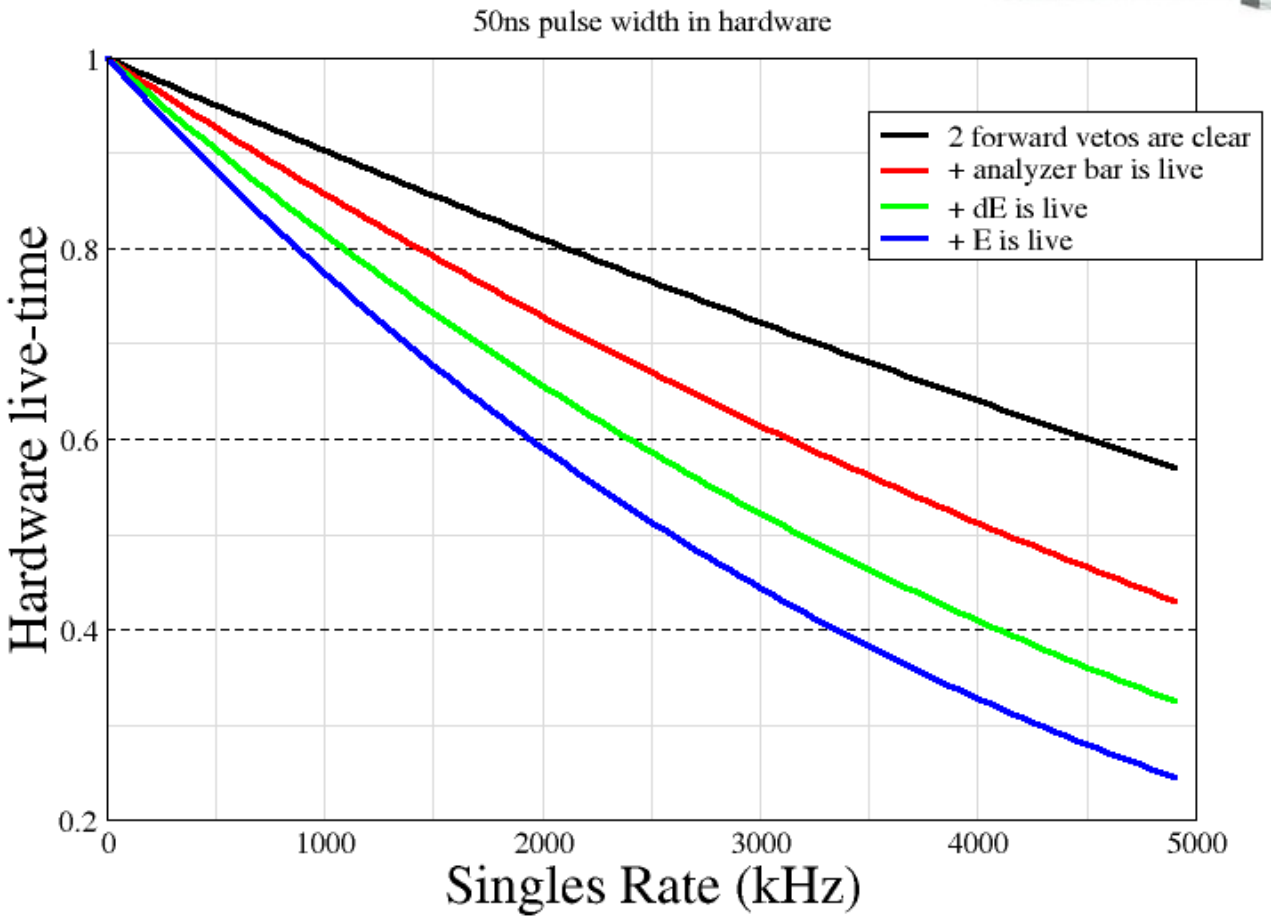
- FASTBUS 1877
  - easily obtainable, good readout speed
  - Resolution: 500 ps/bin
- FASTBUS 1875
  - easily obtainable, less common than 1877s, slow readout speed
  - Resolution: 25 ps/bin
- JLab F1 TDCs
  - Hall C has used these in the past (HKS2), units are scattered but still exist
  - no longer made (Hall D has consumed last run)
  - 32 ch/unit in hi-res mode
  - Resolution: 60 ps/bin
- CAEN v1190
  - most probable candidate for SHMS, HMS
    - can steal modules from HMS
  - Resolution: 100 ps/bin
    - is this sufficient to get desired spacial resolution?
- CAEN v1290
  - some experience with these at JLab, but we would need to buy units for use in Hall C
  - 32 ch/module; $7k/module; (14 units = ~$100k)
  - Resolution: 25 ps/bin

Readout Options: ADC

- FASTBUS 1881 (conventional)
  - easily obtainable, robust, modest readout speed
  - *need a lot of delay cables!*
  - trigger latency starts to matter, *but* FADCs in SHMS help a lot!
  - preferred conventional QDC choice
- CAEN v792 (conventional)
  - VME equivalent to 1881
  - higher speed, less robust under high load than 1881s
- JLab F250 flash-ADCs
  - will be present in both HMS and SHMS (replacing legacy devices)
  - FPGA-based: several output options available
    - total charge (QDC equivalent)
    - full digitized pulse profile (testing/diagnostic use – very high data rate)
    - timing data (optional, probably don't care)
      - 4 ns internal clock, interpolation shown to provide ~1ns resolution or better
  - pipelined device: *no ADC delay lines required!*
  - able to produce a neutron-arm trigger, if desired
    - can replace a large fraction of frontend NIM logic
  - potential long-lead item (can strip HMS for 200 channels)

Deadtime Concerns





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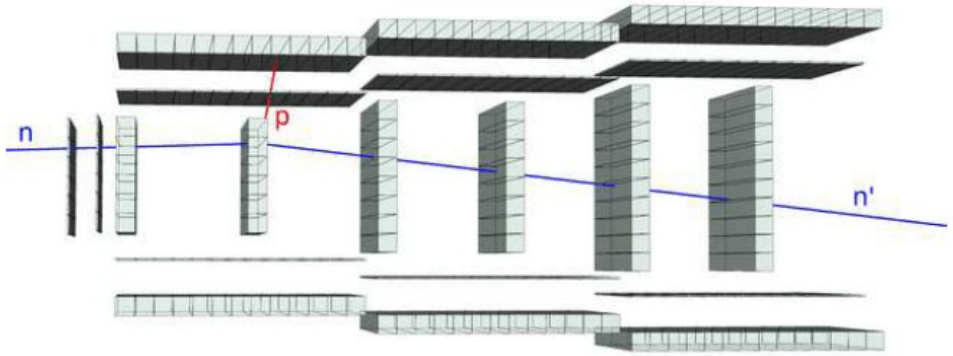

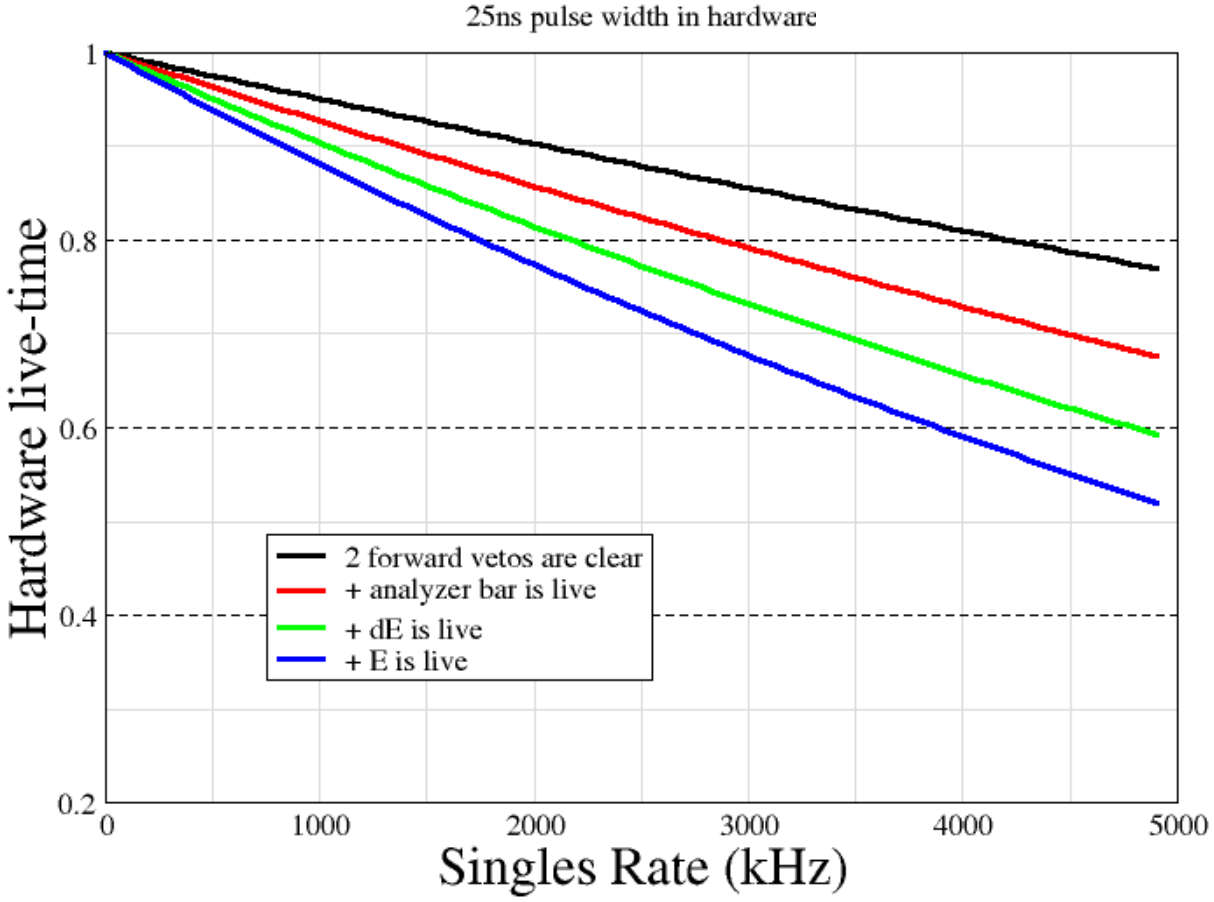

Analyzer Options

- ENGINE (old Hall C fortran code) will be available
  - it will be updated to read-out the new electronics in the SHMS (F250s, CAEN TDCs, etc) in time for 12 GeV startup
  - likely to be relatively stale code by the time we run
- C++/ROOT based analyzer based on the Hall A PODD framework
  - successor to ENGINE, under development now
  - will be ready for first Hall C experiments; will be vetted against the old analyzer
  - modularity built into the OO design (easily extensible)
  - will handle high-rate “blocked” data readout supported by modern electronics (may not apply to us)

Stuff that didn't fit anywhere else...

Miscellaneous Issues

- Beam polarimetry
  - both Moller and Compton will be functional and fully commissioned
  - we can safely assume a dP/P < 3% beam polarimetry without any special effort

Other Questions

- Who's in charge of the target?
  - high power, non-trivial cryo requirements
  - G0: 40cm LH2, 40uA @ 3GeV was spec'd at nominal 500W
  - could be a significant cost, possibly a long lead item
- LED gain monitoring system?
- Custom bases for all forward PMTs?
- Compatibility of magnet placement, shielding hut, etc with new pivot and SHMS carriage