Functional Description of Algorithms Used in Digital Receivers

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***Abstract*—Software defined radio (SDR) systems generally describe transceiver applications; however, the processing requirements of the receiver section are particularly demanding, and require special attention with respect to digital signal processing (DSP). Although the architecture of a digital receiver is closely related to the analog implementation, the numerical operation of each sub-stage can only be realized with fast, efficient algorithms. These include frequency translation, detection, demodulation, filtering, and coding of information for output. This paper analyzes each major subsection of a typical digital diagnostic receiver designed for use in a particle accelerator (without loss of generality), and offers guidance on the implementation and expected performance. An actual SDR platform is presented, with data and analysis.**

***Index Terms*—CORDIC, IIR filter, Nyquist zone, quadrature sampling.**

I. Introduction

SINCE the advent of the superheterodyne (superhet) receiver by Armstrong in 1918, little has changed in the mathematical functionality of the receiver subsections [1]. With the recent introduction of software-defined radios (SDR) for communications and instrumentation, the computational blocks are subject to optimization in ways not possible with respect to conventional mixing, phasing, and filtering. A comparison of some of these techniques provides mixed-signal designers with efficient blocks capable of embedding in microprocessors, digital signal processors (DSP), and field-programmable gate array (FPGA) designs.

II. Receiver Architecture

A. Analog Systems

Extensive analysis and experience has determined that the superheterodyne receiver architecture is superior to other forms, for general use [2]. Although other system topologies may facilitate sub-optimal performance, lower cost, or energy conservation, the superhet is by far the most common.

The canonical radio receiver is based on the ability to obtain a signal, translate the frequency to an intermediate value, and sweep it past a highly selective filter. Subsequently, the signal is then translated a second time, whereby it is detected, and finally demodulated, such that the information can be extracted. This process is depicted in Figure 1, which shows a typical analog superhet receiver, without loss of generality [3].

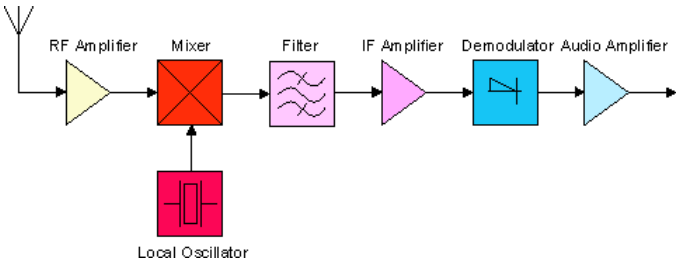

Figure 1. Functional block diagram of a basic superhet receiver, describing major subsystems.

Of interest are the blocks representing frequency translation (i.e. mixer), and demodulation, which also includes the detection operation. Mathematically, the mixer combines the desired signal from the antenna with a sinusoid, and subjects the pair to a nonlinear element. The Fourier analysis of the result consists of a translation involving the sum of the two signal frequencies (the upper sideband, USB), and the difference of the two frequencies (the lower sideband, LSB), along with undesirable cross-terms. In the case of a pure multiplier block, the equations are simply:

$$\sin\theta \sin\varphi = \frac{1}{2}\cos(\theta - \varphi) - \frac{1}{2}\cos(\theta + \varphi)$$

where θ and φ represent the incoming signal and local oscillator (LO) signals, respectively.

Receiver performance is largely determined by how well the pure multiplication is performed, and is described by linearity, or dynamic range. By definition, dynamic range is the ratio of the desired USB or LSB signal and the worst-offending harmonic from the mixing process, described in decibels (dB) [4]. Therefore, a true multiplication has perfect linearity, but is never achievable, in practice. Figure 2 is a depiction of a nomograph of parameters commonly used to describe system and susb-system linearities, and is known as a third-order intercept diagram, since the third-order cross term is usually the most prevalent offending signal, and often resides within the desired signal's passband [4].

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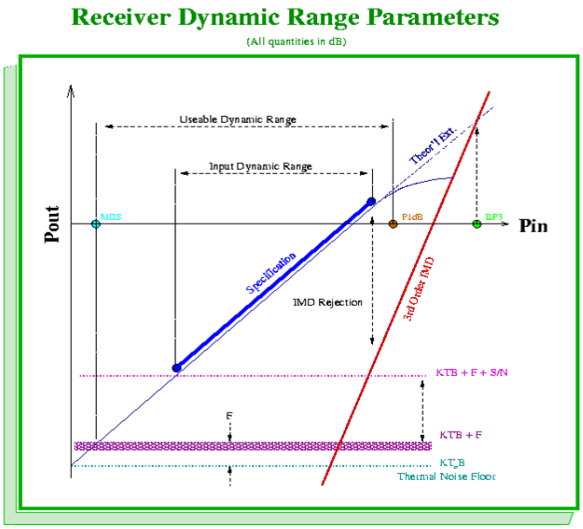

Figure 2. Third-order intercept diagram, often used to determine system linearity. The desired system gain is depicted by the blue line, while the red line demonstrates the appearance of undesired third-order signals from the mixing process, and/or other nonlineraities.

Receiver development has concentrated on minimizing the cross-term production of mixers, but since these are usually constructed from semiconductors or vacuum tubes, only an approximation to the ideal response is achievable.

Signal detection is a function of extracting the amplitude and/or frequency variations from the pure received carrier frequency, prior to the demodulation process. Typical received signals are solely amplitude (AM) or frequency modulated (FM), but also can contain both, as in the case of quadrature amplitude (QAM) or single-sideband (SSB) modulated signals.

AM signals are usually detected using a diode which performs an absolute-value operation, followed by a lowpass-filter. Alternatively, the AM IF signal can be multiplied by a sinusoid of the same frequency and phase, yielding the same result, but with improvement to signal-to-noise ratio [5]. If two quadrature sinusoids (i.e. cosine and sine) are used, the requirement of the LO having phase coherence with the transmitted carrier is removed [5]. In each case, oscillators within the receiver are required to have good spectral purity, minimal amplitude and phase fluctuations, and overall stability.

FM has seen many methods appear for detection, including slope detection, Foster-Seeley discrimination (for wideband FM), zero-crossing detection, and phase-lock loop detection. As in the case of AM, high-quality semiconductor components and chipsets are needed. Also, the demands on oscillators and frequency references are extreme, for high performance [6].

B. Digital Systems

Many of the concepts employed by modern digital receivers have been proposed long before they were practicable, as in the case of the work by Shannon in the early 20th century on Information Theory [7]. As digital systems began to improve in speed and computational agility, so did their ability to realize radio system functions in near real-time. The consequence of numerical replacements for semiconductor approximations is the realization of true multiplication and filter operations, with minimal-to-zero cross-term production.

Although a typical digital receiver system closely resembles that of the analog receiver, the sub-system blocks after signal digitization are numerical, and therefore nearly ideal in performance. The design challenge is shifted from one of component optimization to that of minimizing system latency and maximizing the computational resources of the central processing unit (CPU).

A digital receiver system is shown in Figure 3, for comparison with the analog system [8].

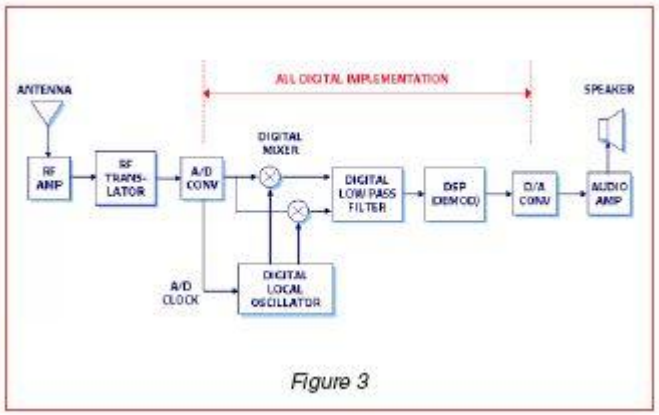

Figure 3. Functional block diagram of a digital receiver system, demonstrating similarity to analog system architecture, but with DSP-specific blocks. All blocks after the ADC are numerically implemented, achieving near-perfect performance.

III. Numerical System Blocks

After an input signal is digitized, it is represented by a fixed-width binary number. In nearly all cases, the subsequent calculations are performed using integer math, as opposed to floating point. This is primarily due to the limited amount of resources available on the CPU, and also to reduce end-to-end latency [9]. Since the ADC is capable of directly outputting twos-complement representations of the input signal (to whatever bit resolution the designer chooses), it is most natural to continue with integer computations; full 32-bit, IEEE representation is not necessary.

A. Quadrature Sampling and Frequency Translation

Since the incoming signal is to be sampled by the ADC, a decision must be made as to the sampling frequency. One choice is to appeal to the Nyquist Theorem, which could (incorrectly) be interpreted to sample at twice the carrier frequency. In reality, the theorem only requires that the sample rate be twice that of the information passband width, regardless of the carrier frequency. However, if the input signal is represented by a spinning vector, a sample frequency of four times the carrier frequency results in an output of the cardinal points (with constant phase offset), X, Y, -X, -Y, … or more conventionally, I, Q, -I, -Q, …where I and Q represent the In-phase (real) and Quadrature (imaginary) components of

the received signal, respectively. Since the amplitude and phase can be obtained by a rectangular-to-polar transformation, the following signal parameters are instantly available:

$$\text{Magnitude} = \sqrt{\text{real}^2 + \text{Imag}^2}$$

$$\text{Angle} = \tan^{-1}\left(\frac{\text{imag}}{\text{real}}\right)$$

Therefore, all of the necessary information is obtained by simply sampling at a 4x rate. A time domain description of the 4x I/Q sampling process is shown in Figure 4, for 70 MHz carrier sampled every 90 degrees.

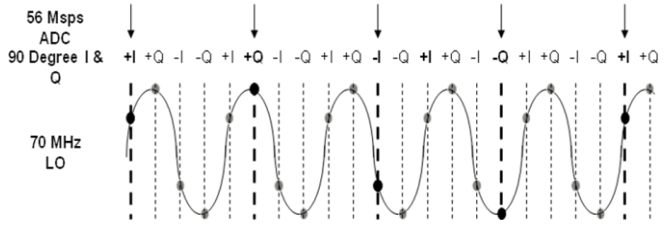

Figure 4. Time-domain description of 4x I/Q sampling process. The output stream contains the rectangular representation of the input signal.

The frequency-domain representation is derived by establishing every combination of:

$$(n\, f_c +/- m\, f_s)$$

Where f_c is the input carrier frequency, f_s is the ADC sampling frequency, and n,m are integers. The next step involves de-multiplexing the stream into the I-only, and Q-only components, resulting in a decimation of 2 (1/2 the sample rate). This stretches the spectra, such that they are nearly touching. Finally, multiplying by alternating +/- 1 produces a positive stream of I and Q values,. And has the consequence of shifting the near-basebend signal by $f_s/2$, such that it is finally centered about DC. Lowpass filtering removes the unwanted frequencies (and replicated spectra), resulting in a baseband, detected signal. The entire process is shown in Figure 5 [10].

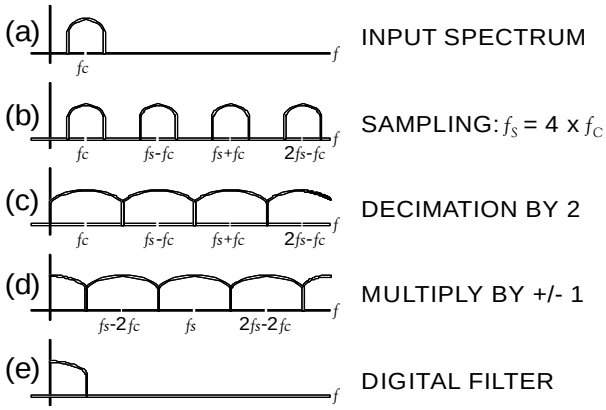

Figure 5. Frequency-domain description of the 4x I/Q sampling process. The original carrier (a) ,with information BW = B, is translated to baseband (b) by the sampling frequency. Decimation stretches the spectra (c), while reducing the data rate. Finally, multiplying by +/-1 sequence and filtering produces a faithful baseband signal.(d).

Although the 4x sampling process is efficient and attractive, the sampling rates required for IF frequencies are extreme for even high-performance processors. Therefore, an undersampling scheme, known as "harmonic sampling," readily exploits the fact that an aliased signal still retains the magnitude and phase relationships of the original signal [11]. As long as the sampling frequency is still larger than twice the information bandwidth, Nyquist criteria are not violated, and the information can be extracted without distortion [12]. In time domain, the concept requires the spinning input vector to over-rotate by either 90 degrees (0.8 f_c), or 270 degrees in between subsequent samples. The slippage results in the same I, Q, -I, -Q,…. sequence, but at a much reduced rate of f_c - f_s. This rate reduction permits the CPU to properly process the input stream, without loss of data. The time-domain description is shown in Figure 6.

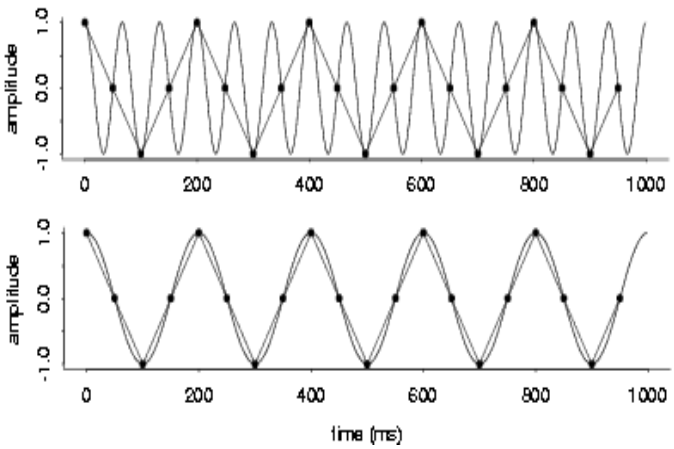

Figure 6. Time domain description of harmonic sampling, whereby the input signal is sub-sampled at a rate of 0.8 f_c , resulting in an aliased signal of f_c - f_s retaining the phase and amplitude features of the original carrier.

As with the oversampled case, the harmonically-sampled IF is translated to baseband through the operation of decimation and multiplication of alternating +/-1. The low-passed result are DC values of I and Q. Spectrally, the process more closely resembles conventional mixing, in that the carrier is translated by the lower-frequency fundamental of the sampling frequency, as shown in Figure 7 [13, 10].

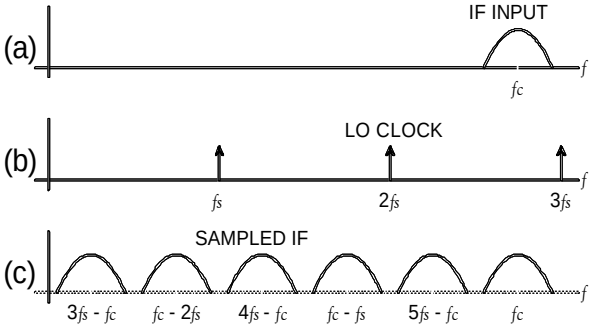

Figure 7. Frequency domain representation of Harmonic Sampling. The carrier is sub-sampled, resulting in a near-baseband representation of the original carrier.

Sub-sampling is not limited to 0.8 f_c rates for the sampling frequency. Theoretically, any (0.8 f_c)/n is permitted, as long as the result is larger than the 2 BW Nyquist rate [12]. However, there is a penalty for extreme undersampling, imposed by the phase noise of the sampling clock. The resulting jitter produces output noise, due to the imprecise sampling instant upon a rapidly changing sine wave, as shown in Figure 8 [6].

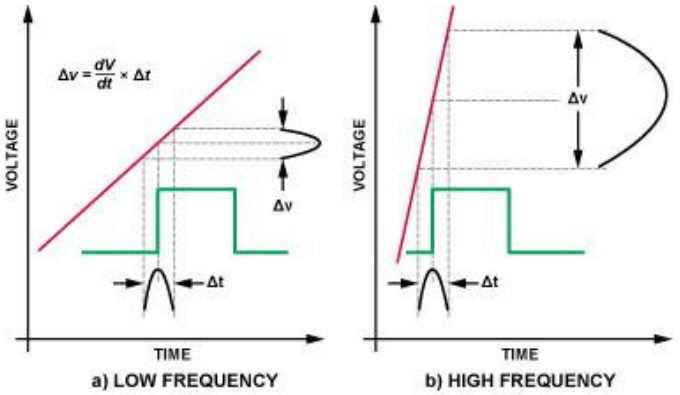

Figure 9. Noise voltage produced from the presence of clock jitter for moderately-undersampled (a) and largely-undersampled (b) cases.

Clock jitter effectively puts a lower bound on the amount undersampling as a function of IF frequency and RMS clock jitter. However, for moderate undersampling, the resulting output rate is generally much larger than the Nyquist rate, which facilitates averaging, known as processing gain. In addition, the quantization noise energy from the ADC process is spread over $f_s/2$, which has the effect of improving the SNR by 10 log (f_s / B), where B is the information bandwidth [14]. Therefore, it is possible to optimize the benefit of oversampling the baseband signal, with the cost of noise generated from clock jitter, which goes as $(f_s/f_s)^2$ [6]. The effect of noise reduction from oversampling is shown in Figure 9.

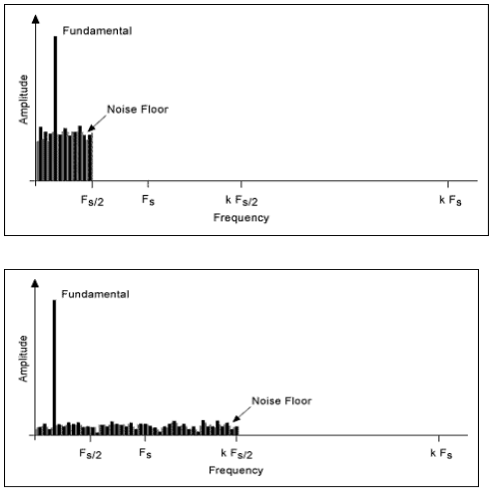

Figure 9. SNR improvement of oversampling baseband. The ADC quantization noise is spread over $f_s/2$, which results in lower overall noise within the passband for higher sample rates.

B. Coordinate Rotation Digital Computer (CORDIC)

Trigonometric evaluations have long plagued both analog and signal processing. Approximations using semiconductors are possible, by exploiting the exponential characteristics of the devices, and Euler's identities. However, the temperature dependence and device variables make this approach relatively expensive with respect to repeatability. Infinite series is attractive for some functions, but convergence and device count are design constraints. For digital systems, the speed of a look-up table is unparalleled, but requires large memory maps if 16-bit (or higher) resolution is needed.

A computational compromise exists with a routine developed in 1959 which iteratively solves a myriad of trigonometric, as well as other linear functions, utilizing a binary search [15]. In this way, it is possible to perform rectangular-to-polar transformations, without having to compute arctan, or the even more taxing sqrt($I^2 + Q^2$). In fact, the algorithm avoids multiply operations, altogether.

The development of the CORDIC revolves around the familiar coordinate rotation matrix [16]:

$$R_i = \begin{pmatrix} \cos\gamma_i & -\sin\gamma_i \\ \sin\gamma_i & \cos\gamma_i \end{pmatrix}$$

If each term is divided by cos γ_i, the matrix becomes:

$$R_i = \frac{1}{\sqrt{1+\tan^2\gamma_i}} \begin{pmatrix} 1 & -\tan\gamma_i \\ \tan\gamma_i & 1 \end{pmatrix}$$

After applying the matrix to the input vector [x y], the system is described by:

$$v_i = \frac{1}{\sqrt{1+\tan^2\gamma_i}} \begin{pmatrix} x_{i-1} & - & y_{i-1}\tan\gamma_i \\ x_{i-1}\tan\gamma_i & + & y_{i-1} \end{pmatrix}$$

Numerically, the tangent terms require a lookup table, followed by a multiply to complete the rotation. However, the process can be further streamlined by examining the mechanics of the binary search algorithm. The strategy lies in rotating the unknown vector such that it lies on the positive real (x) axis. The value of x is exactly the vector's magnitude, while a tally of the rotations yields the original phase angle.

The process begins by rotating the vector by 90 degrees, and evaluating the sign of the resulting y term, sgn(y). If it is negative, over-rotation has occurred, and the next rotation must be in the opposite sense. Otherwise, proceed in the same direction. The next rotation is 45 degrees, followed by 22.5 degrees. The process is repeated b times, where b=number of resolution bits of the input word. So, for a 16-bit input word, 16 iterations are required for the vector-search to converge.

The true utility of the CORDIC lies in the comparison between the tangent of the necessary rotation angles, and the arctangent of the nearest power of ½, as shown in Table 1 [16]. If the tan function can be replaced by a simple division

by 2, then the multiply operation is simply a right-shift, requiring a single clock cycle on all processors.

Table 1. Comparison between CORDIC rotation angles and arctangent of nearest power of ½. The resulting multiplication only requires a right-shift to accomplish.

Angle, γ	Tan γ	Nearest 2^{-n}	$\text{Tan}^{-1}\ 2^{-n}$
45	1.0	1	45
22.5	0.414	0.5	26.6
11.25	0.199	0.25	14.04
5.625	0.095	0.125	7.13
2.1825	0.049	0.0625	3.58
1.4061	0.0246	0.03125	1.79
0.7031	0.0123	0.01563	0.90

Mathematically, the rotation matrix is simplified with the 2^{-n} substitution for the tan function:

$$v_i = K_i \begin{pmatrix} x_{i-1} & - & \sigma_i 2^{-i} y_{i-1} \\ \sigma_i 2^{-i} x_{i-1} & + & y_{i-1} \end{pmatrix}$$

Where σ_i represents the decision rule sgn(y), described earlier, and K_i is known as the CORDIC constant which converges to a value of ~ 1.6 for more n > 5 iterations [16]:

$$K_i = \frac{1}{\sqrt{1 + 2^{-2i}}}$$

Although a lookup table is still required, it contains at most b entries, and is used in a summation role, rather than to perform multiplications. The efficiency of the CORDIC finds its use in many processing environments, and is not limited to trigonometric applications. In addition, the deterministic convergence of b clock cycle iterations makes this algorithm ideal for control-feedback applications, since the latency is absolutely known for every calculation.

C. *Filters*

Because a receiver's performance is primarily a function of SNR, filtering is required at several points in the receive chain, in order to manage thermal noise, and out-of-band interference. DSP filters tend to favor finite-impulse-response (FIR) topologies, due to their inherent stability, and ability to mimic any magnitude response, given enough taps. No feedback is present, thereby controlling number growth within the filter [12]. Drawbacks of such topologies occur when very narrow passbands are needed, or if phase is an issue. In these cases, the extreme number of taps results in unacceptable latency, while the phase control often results in the use of complex coefficients [12].

To avoid these problems, simple feedback filters, known as infinite impulse response (IIR) are often used, since they are reasonably efficient, computationally, and can model typical RLC network responses with respect to phase and amplitude. Drawbacks include possibly instability, as well as large number growth.

Figure 10 compares the FIR and IIR filter topologies.

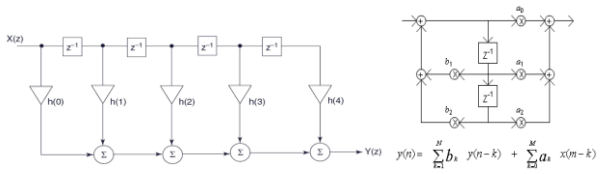

Figure 10. Comparison of FIR and IIR filter topologies, illustrating tap weighting and feedback.

One such IIR topology exploits the divide-by-two concept, thereby removing any multiply operations [17]. The major drawback is lack of frequency control for bandwidths other than powers of 2, but octave resolution is usually sufficient for most narrowband receiver IF filters, and certainly for wider de-noising filters [13]. The filter diagram, and associated bandwidths are given in Figure 11, normalized to a 1Hz input sample rate.

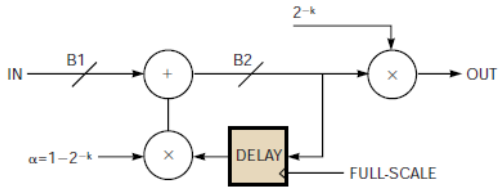

TABLE 1 NORMALIZED BANDWIDTH AND RISE TIME FOR VARIOUS VALUES OF k

k	Bandwidth (normalized to 1 Hz)	Rise time (samples)
1	0.1197	Three
2	0.0466	Eight
3	0.0217	16
4	0.0104	34
5	0.0051	69
6	0.0026	140
7	0.0012	280
8	0.0007	561

Figure 11. System diagram of a novel recursive IIR filter which exploits efficient binary arithmetic (right-shift with add). The associated table provides expected frequency response, normalized to 1Hz input sample rate.

Typical digital receiver topology usually includes a filter immediately following the ADC, in order to begin the noise-limiting, as well as to ensure out-of-band signals are excluded. In addition, copies of the replicated input spectrum must be eliminated, to prevent aliasing. This filter must also be able to begin to extract energy from the signal, and reduce the data rate such that subsequent stages are able to optimize their data-rate-dependent functions [14]. Therefore, a decimating filter is sought, such that the output data is filtered, and has a rate significantly less than the input rate.

A popular input filter which meets these criteria is known as the cascaded integrator-comb filter (CIC). The CIC is simply an accumulator (integrator), followed by a differentiator. The presence of a decimation stage in between the others controls the output data rate, as well as the aggressiveness of the filter [14]. Since the differential basically undoes the effect of the integral, low-frequency coherent signals are unaffected. However, uncorrelated noise is eliminated by the integral, hence improvement in SNR. The computational efficiency is very good for this topology, and only requires sum and difference operations, followed by a single scale factor.

Careful choice of the number of integration, comb, and decimation filters often leads to a scale factor which is a power of 2, requiring only right-shifts. Alternately, other stages can be combined until such a power of 2 is reached within the system, where the right-shift can then be applied. An interesting aspect regarding the integrator is that it is allowed to grow, until the maximum bit representation is reached. In twos-complement systems, the number simply "rolls under." Since the differentiator only cares about the slope of the integration process, overflow is not a concern.

Since the integration can grow without bound, the filter is inherently stable, and easily implemented by the use of a spreadsheet. The topology and typical frequency response are shown in Figure 12.

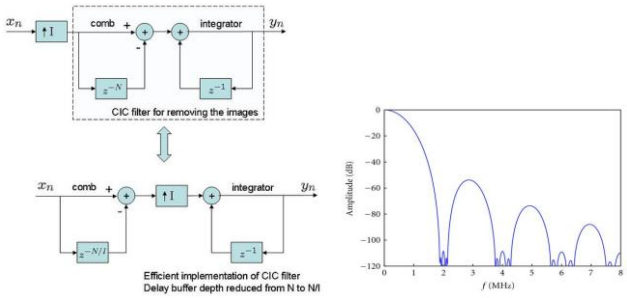

Figure 12. System diagram of CIC filter, showing integration, decimation, and differentiation. Also, a typical frequency response is shown, verifying the effectiveness of the topology.

IV. End-to-End Simulation

A four-channel digital receiver utilizing these numerical concepts was designed and constructed for use as a beam diagnostic system in a particle accelerator [18]. Before actual construction, dynamic modeling was performed using SystemVue, a commercial simulation package which utilizes the popular MATLAB software as an engine [19]. SystemVue enables the designer to construct a mixed-signal system using blocks comprised of data taken directly from data sheets. Digital flow is manipulated with every parameter, and output is easily analyzed using time-domain and frequency-domain tools.

The specifics of the receiver include a conventional heterodyne analog front-end, in order to preserve ultra-low noise figure. The 45 MHz IF is then sampled using a 0.8 rate of 36 MHz, resulting in the alternating I, Q, -I, -Q sequence. Once digitzed, the signal is subjected to a decimating CIC filter, in order to limit the noise energy, extract signal energy, and slow the data rate for subsequent stages.

A narrowband IIR filter, based on the power-of-two design was implemented for ease of configurability, and computational efficiency [17]. Subsequently, a CORDIC algorithm was employed to extract phase and magnitude of the received signal. This signal was then compared to the other channels, in order to calculate the position of the electron beam as it travels down the beam pipe towards the target.

Design parameters include low noise for high resolution, large dynamic range to facilitate a wide scope of beam currents, low latency for control-feedback and machine protection, and affordability for mass implementation.

Figure 13 is a screenshot of the SystemVue model, which contains all non-linear parameters, as well as expected noise components. The three channels represent resonant cavity signals proportional to transverse X and Y beam position, as well as a signal proportional to beam current for amplitude and phase normalization. The inset is the calculated beam position, with respect to cavity boresight.

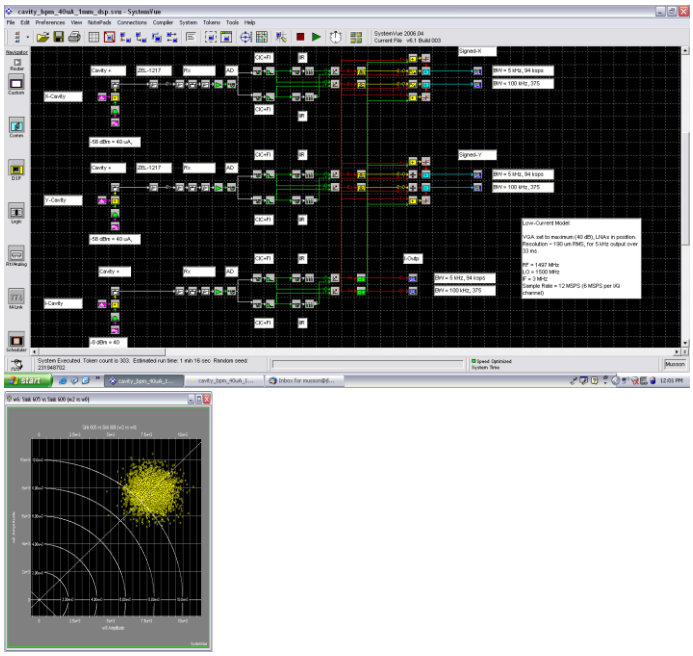

Figure 13. Dynamic simulation of diagnostic receiver, intended for particle accelerator implementation. All parameters representing thermal and system noise elements are included, along with non-linear elements. The inset is the final calculated beam position, with respect to cavity boresight.

Ultimately, the design was constructed and implemented as a SDR, using an Altera FPGA, capable of producing precise beam position estimates with a 100 kHz output rate. In addition, a single-board computer (PC-104) was included as a high-level input-output controller able to perform low-priority high-level applications, such as Fourier analysis, lock-in functionality, and digital storage oscilloscope capability. The receiver performance is shown in Table 2.

V. Conclusion

Numerical algorithms utilized in digital receivers have evolved into powerful computational sub-systems, capable of performing ideal functionality, to within any accuracy. As speed increases, so does the capacity to include more complex arithmetic. The efficiency of the algorithms presented facilitates SDR performance equal to, or better than, conventional analog systems, while providing enormous cost savings and operational flexibility. Also, despite the initial appeal of full floating point math, integer math is fully capable of providing accuracy and precision to any degree, and is naturally compatible with modern ADC systems.

Table 2. Digital receiver (SDR) performance for the beam position monitor application. Actual parameters fell within 3 dB of modeled, validating the simulation.

Quantity (1 Hz BW)		Max Gain	Min Gain
Noise Figure		1.75 dB	2.54 dB
Channel Gain		69 dB	38 dB
Input IP3		-31 dBm	-17 dBm
MDS (ADC- limited)		-143 dBm	-112 dBm
F.S. Input		-59 dBm	-28 dBm
Output Noise Power	1 Hz	-103 dBm	-133 dBm
	100 kHz	-53 dBm	-83 dBm
0.1% THD Range		50 dB-Hz	80 dB-Hz
1% THD Range		70 dB-Hz	100 dB-Hz
(dB-Hz = |MDS| - |20log(THD)| - |IIP3|)			
Signal Level	M15 (4-wire sum)	BCM	Cavity BPM, 1mm
-62 dBm	5 uA	80 nA	3 uA
-112 dBm	17 nA	250 pA	11 nA
-143 dBm	505 pA	8 pA	319 pA

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