



New TDC Development at Jefferson Lab  
Physics Division  
Data Acquisition Group  
Fast Electronics Group  
June 7, 2001

## Motivation:

- LeCroy Fastbus product line discontinued
- Repair and maintenance costs are increasing significantly for Fastbus instrumentation
- Presently no multihit high resolution solution

Will need high resolution multihit TDC to support the new detectors outlined in the 12 GeV Upgrade Plan

Examples:

- Hall A -- Medium Acceptance Detector
  - Drift Chambers
  - Hodoscopes
  - Calorimeter
- Hall B -- CLAS upgrade
  - Central Detector -- Calorimeter, Drift Chamber
  - Forward Tracker
  - Wire chambers
- Hall C -- SHMS
  - Hodoscope Upgrade
  - Wire Chambers
  - Shower counters
- Hall D (8000 high resolution TDC channels)
  - Vertex Chamber/Start counters
  - Forward Tracking Chambers

## The F1 TDC Integrated Circuit

- 8 Channel Time to Digital Converter developed for the Compass experiment at CERN
- Versatile design. Can be configured for 4 high resolution channels or 8 low resolution channels per chip
- *F1* developed at CERN to fulfill the time resolution, multihit, and event rate requirements for the Compass experiment at CERN. *F1* IC developed with industry partner Acam-messelectronic gmbh in Germany. Acam produces the *F1* chip as a commercial product.
- **F1 chip highlights**
  1. Resolution -- Two modes
    - 4 channels--High-resolution 60ps least count.
    - 8 channels--Low-resolution 120ps least count.
  2. Dynamic range -- 16 bits or ~4 $\mu$ S [ High resolution mode ]
  3. Double pulse resolution -- 11nS
  4. On board Hit buffer size -- 32 hits in high resolution mode
  5. On board readout buffer, interface FIFO and trigger count buffer
  6. +5.0 V power
  7. Hit Inputs can be Low Voltage Differential Standard [LVDS], PECL, TTL
  8. 160 pin plastic quad flatpack surface mount device
  9. Commercially available from Acam

More *F1* information on the web at: [http://www.acam.de/Content/F1\\_e.htm](http://www.acam.de/Content/F1_e.htm)



## The Jefferson Lab *F1* TDC Module

Jefferson Lab -- Physics Division --  
Design Team

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### Module Overview

64 input channels

4 front panel connectors. Module will be configured for High-resolution mode (32 channels) or Low-resolution mode (64 channels)

Inputs will accept standard ECL inputs to be compatible with existing systems at JLAB

Additional buffering of each *F1* chip → 32K x 24 bit FIFO

Module memory is 8Mbytes of fast RAM operated as FIFO [ Single VME address ] with 1M x 64-bit organization to exploit the 64-bit transfer mode of VME.

Module will be capable of dual-edge data transfer (2eVME) as defined in the VME64x standard [ Highest data transfer rate ~100Mb/sec]

Module will support "chain-block" transfer for reading multiple TDC modules within one crate.

Can be used in a Non-VME64x powered card enclosure (crate) with provisions on board to produce required 3.3V power.

### TDC Module Comparison

	1872/1875	C.A.E.N. V767	JLAB F1 TDC
Module Format	FastBus	VME; VME (CERN 430)	VME; VME64x
Resolution [LSB]	25ps/50ps/100ps	800ps	60ps/120ps
Channels/module	64	128	32 Hres/64 Lres
Dynamic Range	12 or 15 bit mode	20 bit	16 bit
Double pulse resolution	N/A [Single Hit]	10ns	11ns
Integral non-linearity	< 3 counts	Not specified	<1 count
Commercially available?	Not anymore	Yes	Soon
Multihit?	No	Yes	Yes
Local memory?	No. 8 event buffer	Yes; 32K	Yes: 8M (1M x 64bit)

## Prototype Schedule

- Draft Specification completed April 2001
- Twenty (20) F1 chips have been purchased and received.
- Front end design in progress
  - Channel assignments
  - ECL input configuration
  - Clock stabilization circuits
- VME interface, memory control, CSR interface, and FIFO logic design in progress
- Schematic capture
- Printed Circuit Board layout optimization
- PCB manufacturing
- Assembly
  - Prototype will be assembled in the Fast Electronics Lab with SMD manufacturing equipment
- **Prototype delivery goal by late Fall 2001**
- Testing will present interesting challenges

## Preliminary Cost Estimate [ Prototype quantity of 2 ]

Price per Board

F1 TDC Chips ( 20 chips ) ~\$100/chip	\$800
Memory, Programmable Logic, FIFOs	\$500
Multilayer Circuit Board Manufacturing	\$500
Connectors, passives, front panel, hardware	\$300
Assembly Labor [JLAB]	\$1000
Total	\$3100