

Helicity Clock Generator

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ABSTRACT

Based on the phased-locked loop (PLL) technique, a versatile helicity clock generator has been designed for polarized beam experiments at Jefferson Lab. The module provides synchronized multiple 30, 60, 120 and 61440 Hz helicity clock outputs which are phase-locked with either the AC line voltage or a crystal oscillator. In addition, the Macro Pulse Trigger (MPS) signals required by the G0 data acquisition system are generated from the 60 Hz output through a 250 us adjustable monostable generator.

1. Introduction

A number of polarized beam experiments intend to use a Pockles cell to flip the beam spin with line frequency because the global beam performance such as beam motion and density modulation, is closely related to the line frequency and its higher harmonics. The usual pickup method to trigger the spin flip is to detect the zero-crossing of the AC sine wave with a comparator. Unfortunately, near the zero-crossing point, there is a certain amount of circuit noise that generates pickup jitter. When the line signal is distorted the pickup jitter becomes larger. To solve this problem and provide a more accurate spin flip trigger we developed a circuit based on the a PLL design (fig. 1).¹

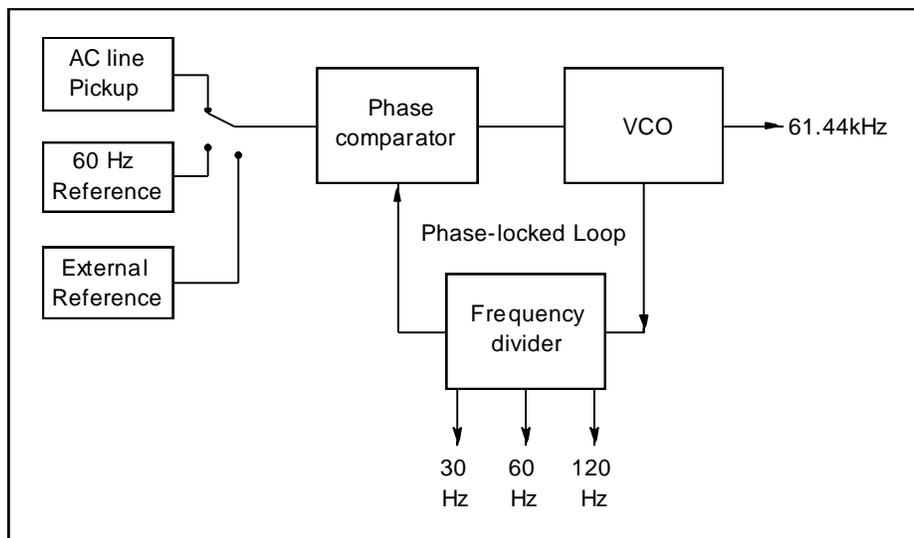


Figure 1: Block diagram of the helicity clock generator.

As shown in the figure, there are 3 options for the reference signal controlled by a three position switch. In the first option, a 60 Hz clock can be easily generated from a line pickup

circuit. In this way, 60 Hz clock is exactly synchronized with the power line. Another option is using a crystal oscillator. The crystal oscillator generates a 600 kHz master clock signal which is divided to produce a 60 Hz clock with 100 ppm stability. The last option is an external BNC input. This front panel switch can be set according to the needs of experiment. For the G0 experiment, a fixed frequency of helicity clock is required in which case the switch should be set to the crystal oscillator lock.² In this case, there is slow phase slip between line and the outputs.

This reference signal is then sent to a phase comparator which controls a voltage controlled oscillator (VCO) which produces a 61.44 kHz output frequency. This output is divided down to 60 Hz and feed back to the phase comparator to lock in the frequency. This frequency lock provides great immunity from any AC line distortion or from transmission noise of any external 60 Hz reference inputs. The output from this module is four parallel synchronized output frequencies; 30, 60, 120, and 61440 Hz phase locked to the input reference frequency.

2. Circuit diagram and description

Figure 2 shows the circuit diagram of the clock generator. At the AC input terminal, a low-pass EMI filter is used to remove all the relatively high noise present on the 60 Hz power line signals. The pickup circuit is based on the 555 timer chip.³ The two input comparators of the 555 are connected as a discriminator. The upper threshold is fixed at 2/3 of the power supply voltage while the lower threshold is fixed at 1/3 of the power supply voltage. This type of Schmidt trigger has a very high hysteresis that forces pickup noise down to a minimum and produces the 60Hz trigger to the PLL section.

For the second option, a single chip 8640AN crystal oscillator is used to generate a 60 Hz clock frequency. The master crystal oscillator produces 600 kHz clock with 100 ppm accuracy which is followed by a down-counter chain to generate a 60 Hz output. Due to the asynchronization with line frequency, there is slow phase slip between line and PLL output 60 Hz clocks.

As one of the most common applications of PLLs, we use a 4046B PLL chip to generate a fixed multiple of the 60 Hz input frequency.⁴ The 4046B phase detector is connected in edge-triggered mode (type 2) due to its simplified loop filter. The output of the phase detector is fed to the on-chip VCO to produce an integer multiple (1024) of the 60 Hz reference signal. The unique virtue of such a PLL scheme gives infinite rejection of 60 Hz pickup present on any signal input to the converter. The distortion of the line signal and the pickup noise near the zero-crossing point are fully eliminated by this PLL.

The 61.44 kHz output from the PLL is fed to a 4040 division counter. This divides the frequency by 1/512, 1/1024, and 1/2048 to produce output frequencies of 30, 60, and 120 Hz. The 60 Hz output is fed back to the 4046B PLL to complete the loop and lock the frequency. Thus we obtain 4 parallel synchronized output frequencies: 30, 60, 120, and 61440 Hz phase locked with the input reference frequency.

Due to the sensitivity of the 4046 to variation in its supply voltage, we also developed a stabilized power supply based on the LP2950 powered by the AC input voltage. Careful design of the LP2950 has minimized all contributions to the error budget. This includes a tight initial tolerance (.5% typical) and extremely good load and line regulation (.05% typical).

The MPS (macro-pulse trigger) signal is produced from a one shot which shapes the 60 Hz clock into 250 μ s trigger pulse. In order to flip the beam spin, the Pockels Cell of the injector

needs at least a 250 μs settling time for both spin orientations. The data acquisition gate will the open for the remaining 16.4166 ms time interval.

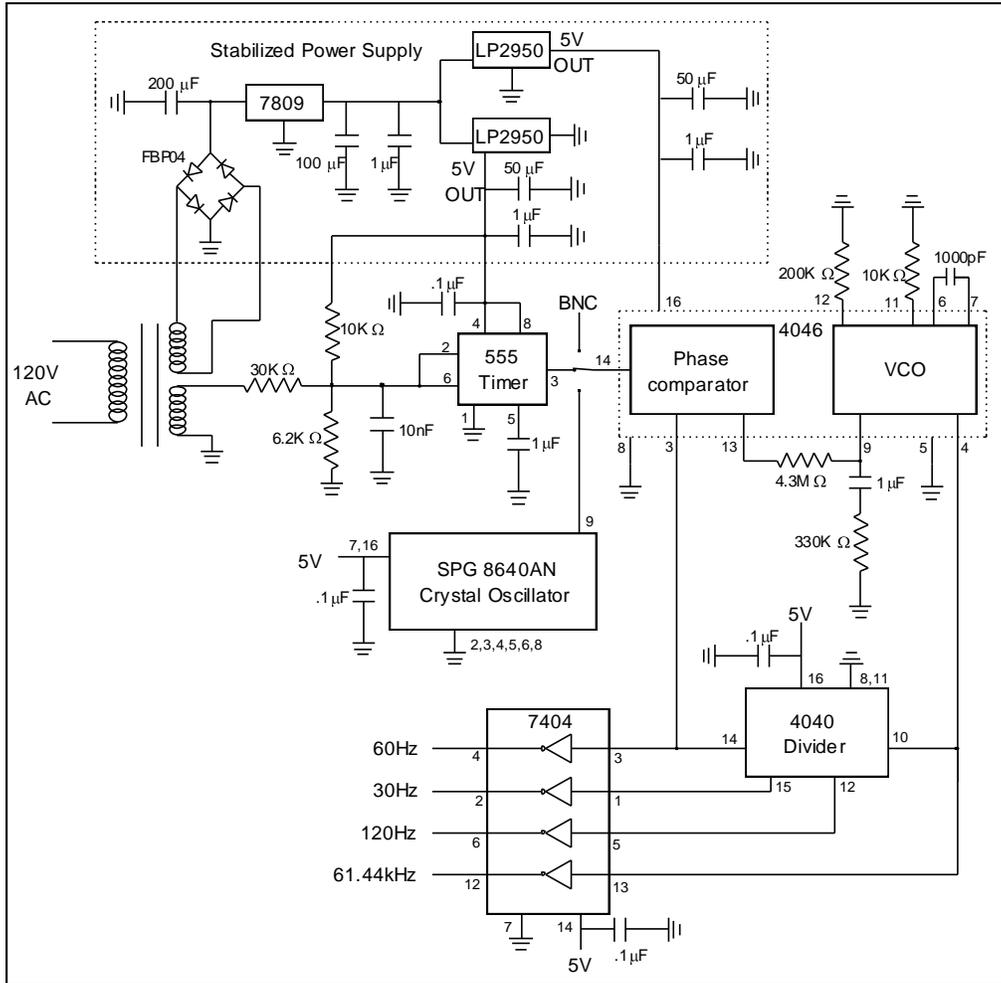


Figure 2: Circuit diagram of the helicity clock generator.

3. System performance

A picture of the generator connected to an oscilloscope is shown in figure 3. The output waveforms from the PLL in AC line-phase lock is shown in Figure 4. The AC line reference signal waveform is displayed on the top of the plot with the 60 Hz and 30 Hz outputs displayed below. At the bottom of the picture is the MPS signal.

The circuit was tested with a quantitative simulation of the input signal fluctuation using a WAVETEK DDS function generator. The WAVETEK generator was set to Frequency Shift Keying (FSK) mode - permitting fast phase-continuous switching between two frequencies. The performance of the PLL module was tested with the difference of the two frequencies set to 10^{-3} level. With the FSK off, the phase jitter of the 4046B PLL is about 4 μs , corresponding to 0.01 mrad . With the FSK on, the catch time of the PLL is about 1 second and the maximum phase shift is about 20 μs (set differential ratio $df/f = 10^{-3}$).



Figure 3: Picture of helicity generator setup.

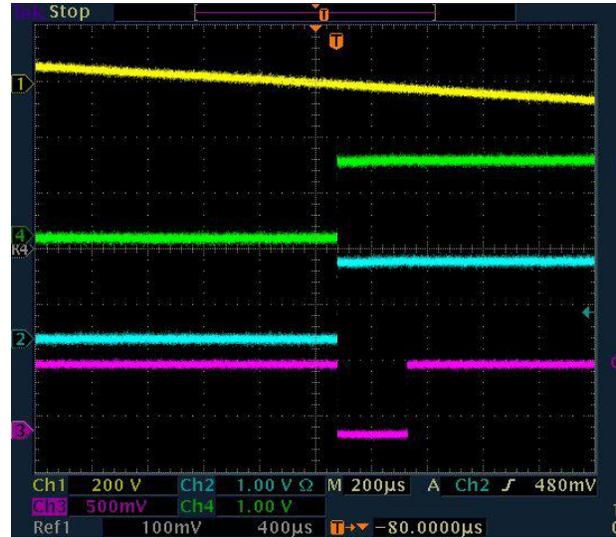


Figure 4: Waveforms from the helicity generator. The left image shows (from top) the AC reference signal, 60 Hz output, 30 Hz output, and MPS signal at 4 ms/div. The right image shows an expanded time view at 200 μ s/div.

4. Reference

1. Paul Horowitz, "The art of electronics"

2. Mark Pitt, Helicity Control Request from G0 Experiment March 22. 2001
3. 555 application notes
4. 4046B application notes