Electronics for the HKS – ENGE Hypernuclear Spectrometer System

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Abstract

This document describes the general electronics layout and trigger philosophy for the HKS spectrometer system

1 Introduction

The HKS – ENGE Hypernuclear Spectrometer System consists of one hadron spectrometer for the detection of kaons (HKS) and one electron spectrometer (ENGE). The associated focal plane instrumentation is very similar to the one that has been employed in E89-009 (HNSS). During HNSS running the electron arm (ENGE) rate was so high that each kaon event was associated with up to 8 electron events (within a reasonable coincidence time window). Therefore, a coincidence trigger was not feasible and the data acquisition (DAQ) has been triggered by the kaon arm alone. The HKS-ENGE system, however, will operate the ENGE spectrometer tilted out-of-plane with respect to the splitter magnet. This will largely reduce the background rate associated with bremsstrahlung and Moeller electrons. The total electron rate should be no larger than 5 MHz. The hadron arm rate is assumed to be no more than 1.5 MHz (1 MHz π^+, 500 Hz K^+, and 0.5 MHz proton). This will allow to run the DAQ with a electron-hadron coincidence trigger. The total trigger rate should be kept below 1 kHz. Therefore, particle identification (PID) on the trigger level has to reduce the pion and proton rates to 1×10^{-4} and 5×10^{-4}, respectively. To reduce the likelihood of accidental kaon vetoes due to multiple tracks, the hadron trigger will be segmented.

1.1 General Strategy

High Voltage to all detectors is supplied from the CAEN crates on the second floor of the counting house. These crates have been installed to supply the G0 detector. Bundled cables, each consisting of 16 HV lines, run from the second floor to a patch panel on the left side in Hall C. The lines terminate in 16-fold connectors, used by G0, and in addition in individual SHV jacks. The G0 connectors will be unplugged and HKS will utilize the SHV jacks. From there RG59 cables will run to the two detector huts. HV settings will be controlled with the EPICS slow control system from the Hall C counting room.

TDCs: All wire chambers will use the newly developed F1 multi-hit TDC in low resolution mode, 64 channels per module. The ENGE hodoscopes will use the F1 TDC in high resolution mode, 32 channels per module. All F1 TDCs will be housed in VME crates in the respective detector huts. The HKS hodoscopes, requiring the best possible timing resolution, will be read by LeCroy LRS1875 TDCs set to 25 ps/channel. The LRS1875 will be housed in Fastbus crates in the Hall C counting room.

Delay lines: All ADC signals and the TDC stop signals for the HKS hodoscopes need to be delayed until after a valid trigger is formed. For this, as much as possible, the existing HMS/SOS delay lines will be employed. These lines are approximately 400 ns long.

1.2 Electron Arm (ENGE)

The instrumentation for the electron arm consists of a honeycomb drift chamber and a scintillator array. The scintillator array has two planes with 25 segments each and in the back one additional scintillator covering the entire focal plane for cross calibration of the two front planes. The scintillators provide the electron trigger and the start time for the drift chamber. Due to the high anticipated electron rate a segmented trigger scheme is employed.

1.3 Kaon Arm (HKS)

The instrumentation for the hadron arm consists of drift chambers for tracking, scintillators for trigger and time-of-flight, and aerogel and water Čerenkov detectors for particle identification. For high particle rates, the trigger can be segmented in up to 6 groups. This prevents scintillator triggers from one section of the focal plane from being suppressed by PID signals from a different section.

2 ENGE Spectrometer

2.1 ENGE Scintillators

The electronics layout is shown in Fig. 1. A breakdown of the timing is given in Table 1.

The Hamamatsu H6612 assembly has two short, approx. 30 cm long cables for signal and HV attached directly to the assembly. The signal cable ends in a Lemo plug, the HV cable in a SHV connector **(Need to identify whether plug or jack. In case of plug need adapter or jack on cable.)**. The applied potential is roughly -1450V. To provide for adequate strain relief, it is suggested to mount

ENGE Scintillators (F1 TDC downstairs)

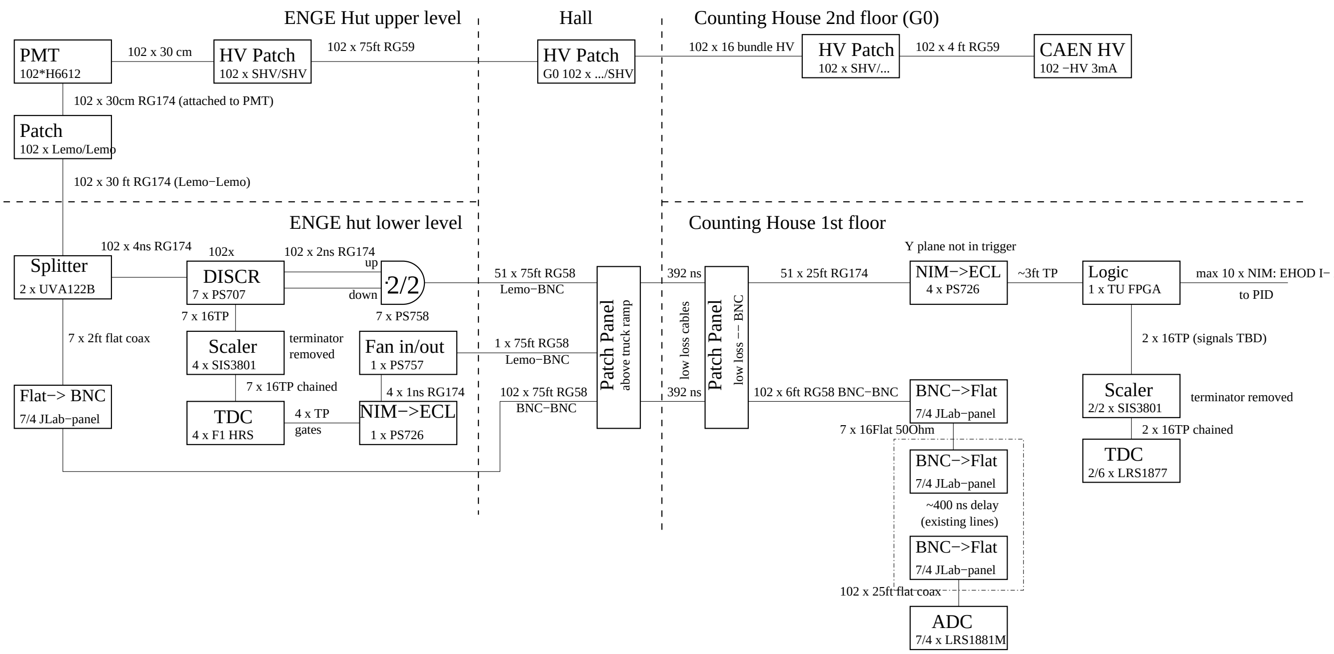

Figure 1: ENGE scintillator electronics. See text for details.

two patch panels right above and below the detector (or maybe one behind). From this patch panel, 30ft RG174 (Lemo—Lemo) carry the signals from the detector level to the ground level of the hut. There the signals are split by **UVA 122B signal splitters or a dedicated splitter (Lemo in/Lemo& BNC out)** for TDC/Trigger and ADC processing:

ADC: If UVA splitter, then short 16 pair flat coaxial cables connect to a JLab Flat—BNC panel. From this panel 125ft RG58 connect to the patch panel above the truck ramp. In the counting house RG58 (BNC-BNC) connect to a JLab BNC-Flat panel. From there flat coaxial cables (50 Ω) connect to the existing 400 ns delay lines. These delay lines are RG58 cables connected at in- and output to JLab Flat-BNC panels. **(Still need to verify the exact delay.)** After the delay, 25 ft 16 pair flat coaxial cables connect directly to the LRS1881M ADCs.

TDC/Trigger The second output from the splitter connects with 4 ns RG174 (Lemo—Lemo) to Phillips PS707 discriminators. This discriminator is a custom designed module that has one NIM and one ECL output per channel. From the ECL output, 17 pair twisted pair cables are chained to SIS3801 scalers and JLab F1 TDCs. The terminators in the SIS3801 should be removed. **Optional, the scalers could also be located in the counting house and count the "up"&"down" coincidences. In any case, it should be verified that chaining the scalers to either the F1**

TDCs or the TU FPGA does not negatively effect the performance of the TDCs or FPGA. The second discriminator output connects via RG174 (Lemo—Lemo) to Phillips PS758 logic modules that form the logic `.AND.` of the top and bottom tubes. From here on the signal path to the counting house is identical to the analog signals, except that the 75 ft RG58 have Lemo connectors on the hut end and BNC on the patch end. From the counting house patch, 25 ft RG174 (BNC—Lemo) carry the timing signals across the room to Phillips PS726 NIM—ECL converters in the 3rd-arm racks. Two 3 ft 17 pair twisted pair connect to the TU FPGA logic module. The FPGA forms coincidences between the front and back plane in up to a maximum of 10 groups (limited by the 10 NIM outputs of the FPGA module.) Alternatively, more sophisticated grouping could be achieved within the FPGA and only one trigger signal being extracted for trigger purposes. In contrast to the HKS detectors, grouping in the ENGE hodoscopes serves only the purpose of reducing accidental coincidences between the front and back plane.) Up to 32 signals can be extracted from the ECL outputs and recorded by scalers and low resolution TDCs for efficiency studies.

Table 1: ENGE scintillator timing. See text for details. For the timing between Hall C patch panels see Section **??**

RG58 Speed	0.64
Flat Coax	0.64
Twisted pair	0.64

EHODO Timing

Target-detector	15.0
Detector transit	0.3
H6621 transit	19.0
30 cm RG174	1.6
Patch	0.0
30 ft RG174	46.9
UVA Splitter	0.0
Total target-splitter	**82.7**

ADC

Target-splitter	82.7
2ft flat coax	3.1
Flat-BNC	0.0
125 ft RG58	195.3
truck—above patch	122.5
Above pat-Hall pat	19.0
Hall patch-CH	250.0
Xx ft RG58	400.0
BNC-Flat	0.0
25 ft flat coax	39.1
Time @ ADC	**1111.7**

TDC

Target-splitter	82.74
RG174	4
PS707	9.5
Xx ft TP	10
Time @ TDC	**106.24**

Trigger

Target-splitter	82.74
RG174	4
PS707	8.5
RG174	4
PS758	8
125 ft RG58	195.31
truck—apatch	122.5
apat—Hall pat	19
Hall patch-CH	250
25 ft RG174	39.06
PS726	5
3 ft TP	4.69
FPGA	50

2.2 Honeycomb Drift Chamber

The electron arm has one honeycomb drift chamber, HC1 with approx. 1200 channels. HV is supplied via 5 RG59 cables at a potential of roughly -2200V. The anode wires are read out by 70 Nanometric amplifier discriminator cards (see Section **??**). Each card reads 16 channels. The power consumption per card is 5.4 W (+5 V, 0.4 A, and -5 V, 0.68 A). The low power supply (Acopian???) needs to provide at least 28 A at +5 V and 48 A at -5 V. The discriminator threshold is set by an external voltage provided by a BK Precision 1660 power supply, located in rack CH03B10 in the electronics area of the counting house. The optimal threshold at the operating point of the chambers is $x.yy$V. This is set with a dial on the front of the device. Each discriminator output is connected by 34-pin (17 pair) twisted-pair cable to a JLab F1 TDC with 64 channels per module in low resolution mode (18 modules). The TDCs trigger signal is distributed via a fan-out and NIM-ECL converters.

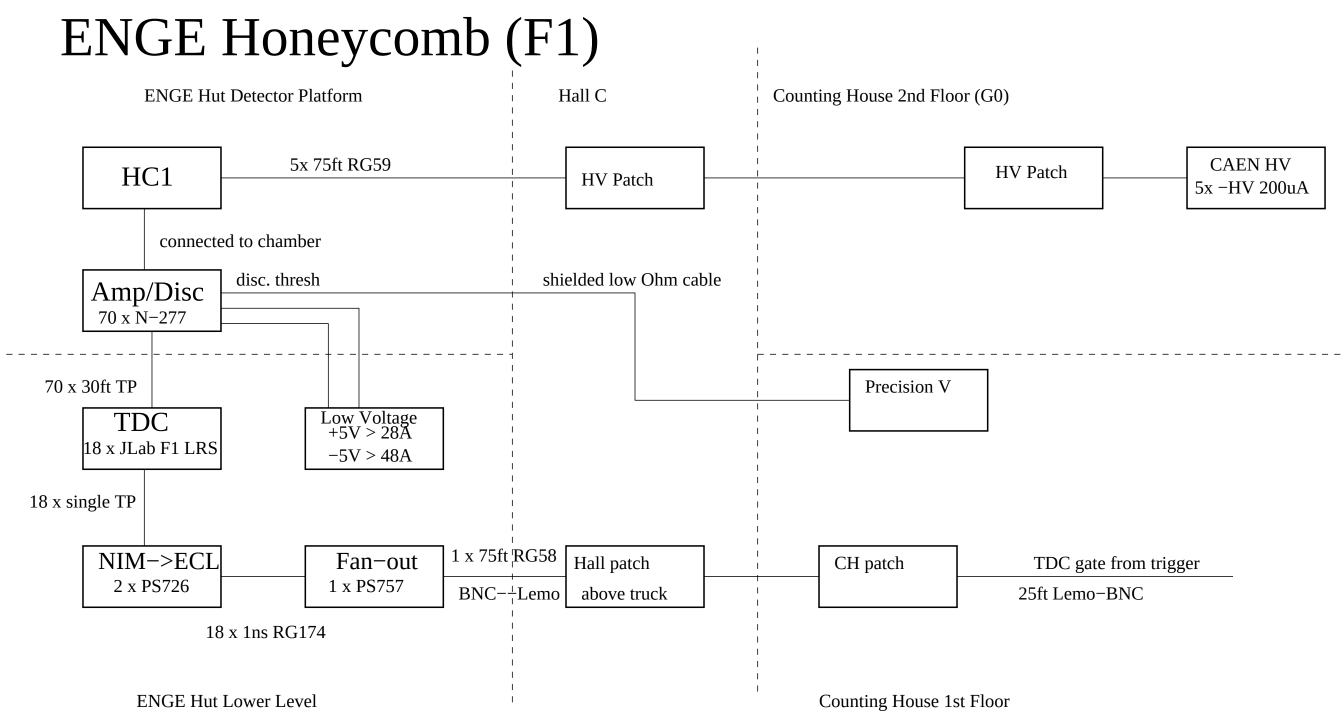

Figure 2: ENGE honeycomb electronics.

3 HKS Spectrometer

3.1 Scintillators

There are three scintillator planes, HS1, HS2, and HS3. HS1 consists of 17 vertical (x) segments, HS2 of 9 horizontal (y) segments , and HS3 of 18 vertical (x) segments. Each segment has two tubes; top and bottom for HS1 and HS3, left and right for HS2. They are named HS1T1 ... HS1B17, HS2L1 ... HS2R9, HS3T1 ... HS3B18. T1/B1 is left (positive spectrometer x) and T17/B17 is right (negative x) when viewed from downstream. Top & bottom counters #1 are at negative spectrometer x and counters #25 are at positive spectrometer x. Left counters are at negative and right counters at positive spectrometer x, respectively. For the horizontal layer, HS2, left and right counters #1 are low and #9 are high.

The electronics layout is shown in Fig. 3. The Hamamatsu H1949-50 2inch photomultiplier tube assemblies have two anode outputs. One output is send directly to the counting house where it is recorded by an ADC. The second output is discriminated in the detector hut and then send to the counting house. In the counting house, the timing signals are discriminated again to compensate for cable losses and dispersion. From the discriminator, signals are send via delay lines to high resolution TDCs and a second branch to TU FPGA logic modules. The logic forms the mean time of each pair of PMTs and further provides the possibility for segmented coincidences between front and back planes. For the horizontal layers, H2, a simple logic `.OR.` is formed. Signals from each stage of the logic are send to low resolution TDCs and scalers.

3.2 Aerogel Čerenkov

There are three layers of aerogel detectors, HA1, HA2, and HA3. Each layer has 7 segments. Each segment has two tubes; top and bottom. They are named HA1T1, HA1B1, ... , HA3T7, HA3B7. Counters #1 are at negative spectrometer x and counters #25 are at positive spectrometer x. All aerogel electronics and HV supplies are upstairs in the counting house.

3.2.1 Aerogel PMTs

The aerogel detectors use two different types of photomultiplier tubes, Hamamatsu R1250 and Photonis XP4572B/D1. Both types are operated in a kathode ground scheme (positive HV to anode). The Hamamatsu R1250 use voltage dividers built at FIU. The Photonis XP4572B/D1 use the Photonis VD305 voltage divider with an additional amplifier built at JLab added diretly into the divider housing. The amplifier does not require a low voltage supply; it gets its power from the last stage of the voltage divider.

The PMT anode signals are directly connected with 125 ft RG58 (BNC-BNC) to the Hall C patch panel. In the counting house, the signal first runs through a splitter (or linear fan in fan out). One branch gets delayed by ≈ 400 ns and goes to the ADCs. The second branch goes to discriminators

HKS Scintillators

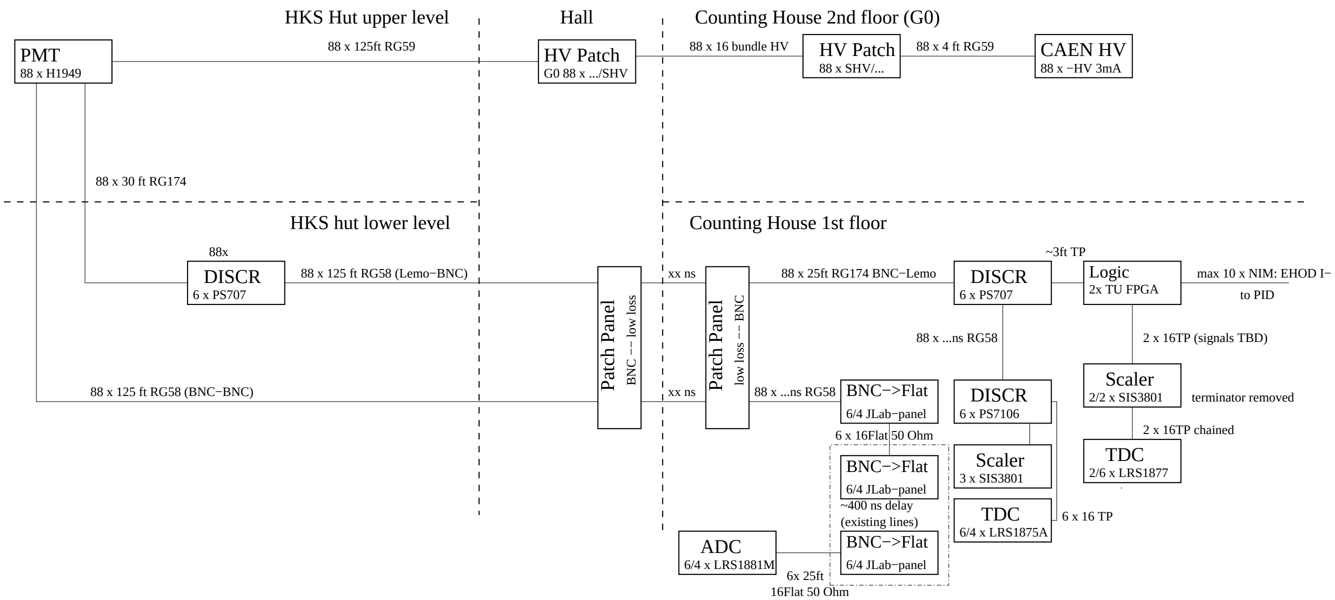

Figure 3: HKS scintillator electronics

HKS Aerogel Cerenkov

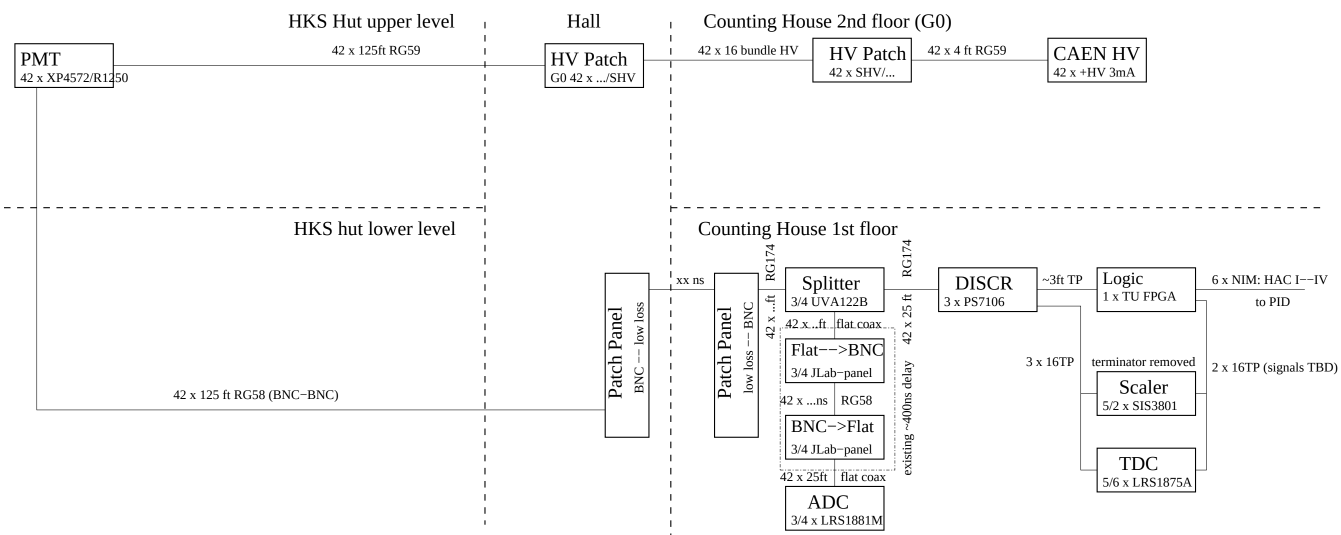

Figure 4: Aerogel trigger for segmented pion veto

Table 2: Aerogel PMT characteristics

tube	HV	Gain	Rise time	Half width	Transit time
XP4572B/D1	2100 V	2×10^7	4.3 ns	5.5 ns	48 ns
R1250	3000 V	1.4×10^7	2.5 ns	—	54 ns

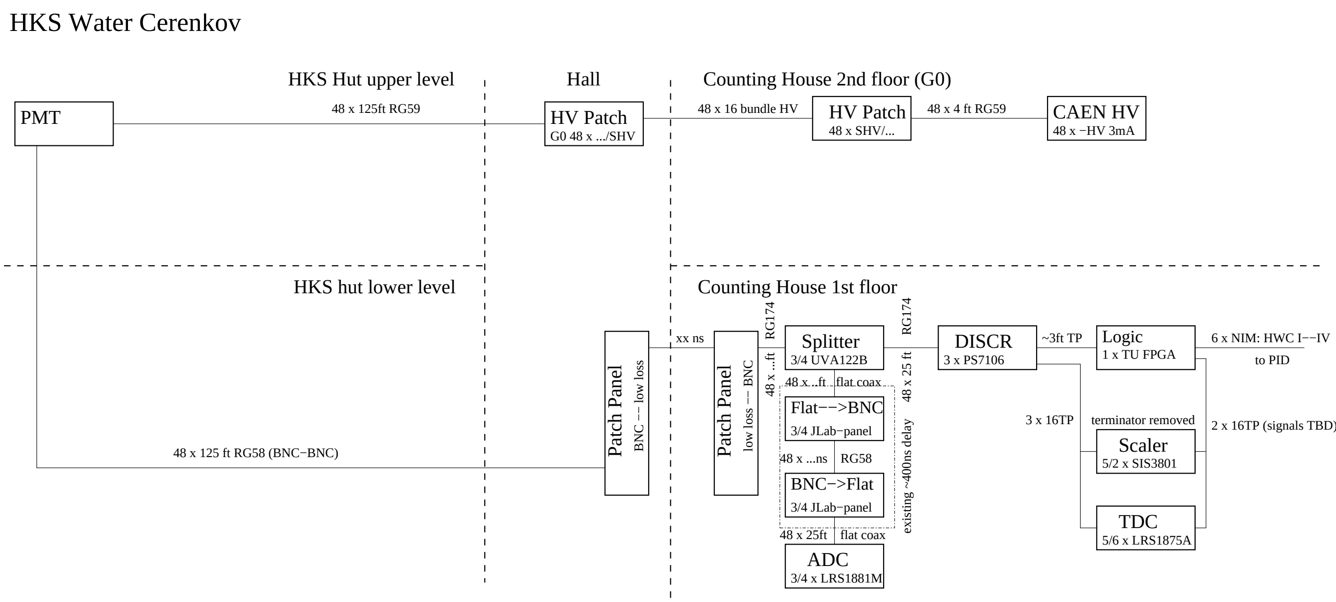

Figure 5: Water Čerenkov trigger for segmented kaon trigger

(either PS707 or PS7106) in the 3rd arm rack. One Tohoku University FPGA module forms the desired logic (.AND. and segmentation). The discriminated signals before the logic as well as up to 32 signals after the logic are send to scalers and low resolution TDCs for trigger studies.

3.3 Water Čerenkov

There are two layers of water Čerenkov detectors, HW1, HW2. Each layer has 12 segments. Each segment has two tubes; top and bottom. They are named HW1T1, HW1B1, ... , HW2T12, HW2B12. Counters #1 are at negative spectrometer x and counters #12 are at positive spectrometer x. All water Čerenkov electronics and HV supplies are upstairs in the counting house.

The electronics layout is shown in Fig. 5. It is essentially the same as for the Aerogel Cerenkov.

3.4 Drift Chambers

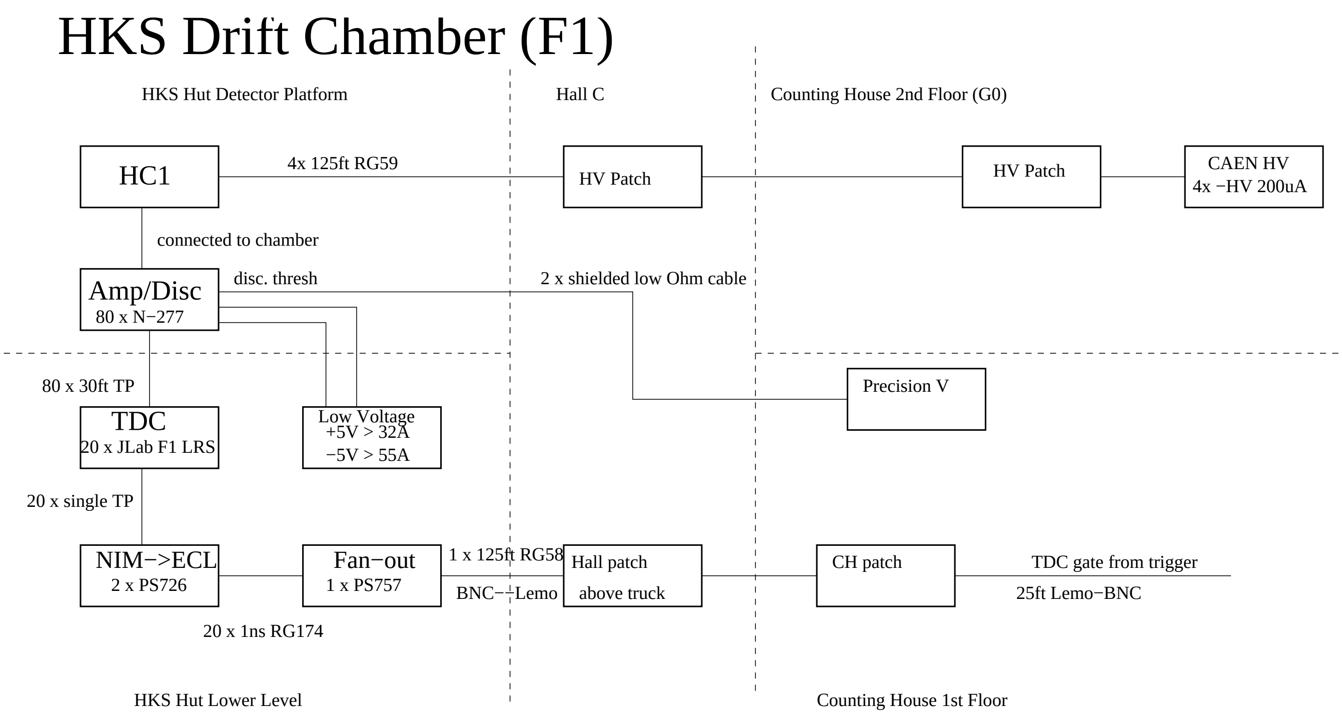

Figure 6: HKS drift chamber electronics.

The kaon arm has two drift chambers, each with roughly 650 channels. They are read out by a total of 80 Nanometric amplifier discriminator cards (see Section **??**). Each card reads 16 channels. The power consumption per card is 5.4 W (+5 V, 0.4 A, and -5 V, 0.68 A). The low power supply (Acopian???) needs to provide at least 32 A at +5 V and 55 A at -5 V. The discriminator threshold is set by an external voltage provided by a BK Precision 1660 power supply, located in rack CH03B10 in the electronics area of the counting house. The optimal threshold at the operating point of the chambers is $x.yy$V. This is set with a dial on the front of the device.

3.4.1 Drift Chamber Readout

Each anode wire has its own electronic readout through Nanometrics preamplifier/discriminator cards (or LeCroy Corporation LRS 2735DC cards which are interchangeable with the Nanometrics cards). Each of these Drift Chamber cards has 16 inputs which accept negative signals from the anodes (sense wires), amplify and then digitize the signals according to whether a user-specified threshold level is crossed. This threshold level is set using a low voltage (0 to 10 volts) dc power supply. A multi wire cable connects this threshold power supply to the Drift Chamber cards. Each of the Nanometrics or LRS cards requires approximately five volts (bipolar) and approximately 1/2 A. This power is supplied by Acopian supplies. Each discriminator output is connected by 34-pin (17 pair) twisted-pair cable to F1 TDCs with 64 channels per module in low resolution mode.

4 Trigger

5 Fission Chamber

6 List of all electronics/cables

	EHD	EDC	HHD	HAC	HWC	HDC	PID	Trg	Sum	Have	Need
Cables											
RG59 75ft ??	102	5							**107**		-107.00
RG59 125ft ??			88	42	48	4			**182**		-182.00
RG174 25ft Lemo-Lemo	51	1	88	42	48	1			**231**		-231.00
RG174 30ft Lemo-Lemo	102		88						**190**	310	120.00
RG58 6ft BNC-BNC	102		88						**190**		-190.00
RG58 75ft Lemo-BNC	54	1							**55**		-55.00
RG58 75ft BNC-BNC	102								**102**	300	198.00
RG58 125ft Lemo-BNC			88			1			**89**		-89.00
RG58 125ft BNC-BNC			88	42	48				**178**	200	22.00
RG174 1ns	4	18				20			**42**		-42.00
RG174 2ns	102								**102**	200	98.00
RG174 4ns									**0**	280	280.00
RG174 8ns									**0**	220	220.00
ECL 30ft		70				80			**150**	200	50.00
16xCoax 2ft	14		6						**20**		-20.00
16xCoax 25 ft	7		6	3	3				**19**		-19.00
CH-Hall Patch 50 Ohm			176	42	48	1			**267**		-267.00
CH-Truck Patch 50 Ohm	154	1							**155**		-155.00
CH G0-Hall G0 HV	102	5	88	42	48	4			**289**		-289.00
Shielded low Ohm		1				2			**3**		-3.00
RG58 400ns Lemo-Lemo			88						**88**		-88.00
Connectors											
Lemo for RG58	54	1	88			1			**144**	200	56.00
BNC/Lemo	51	1	88			1			**141**	200	59.00
Twisted Pair 34 pin	35	140	18	21	21	160			**395**	600	205.00
Panels											
UVA 122B Splitter	2			3/ 4	3/ 4				**3 1/ 2**		-3.50
Flat Coax/BNC Panel	4		2						**6**		-6.00
32 x 400 ns delay	3 1/ 2		3	1 1/ 2	1 1/ 2				**9 1/ 2**		-9.50
NIM Modules											
NIM crate									**0**		0.00
PS707 Discr	7		12						**19**		-19.00
PS757 Fan out	1	1				1			**3**		-3.00
PS726 NIM/ECL	5	2				2			**9**		-9.00
PS758 Logic	7								**7**		-7.00
CAMAC Modules											
CAMAC crate									**0**		0.00
PS7106 Discr			6	3	3				**12**		-12.00
VME Modules											
VME crate									**0**		0.00
VME CPU									**0**		0.00
SIS3801 Scaler	5		4	2.5	2.5				**14**		-14.00
F1 TDC low res		18				20			**38**		-38.00
F1 TDC high res	4								**4**		-4.00
TU FPGA	1		2	1	1				**5**		-5.00
Fastbus Modules											
Fastbus crate									**0**		0.00
LRS1875/72 TDC			2						**2**		-2.00
LRS1877 TDC low res	1/ 3		1/ 3	5/ 6	5/ 6				**2**		-2.33
LRS1881M ADC	2		2	1	1				**6**		-6.00
High Voltage Supply											
SY403 HV crate	1 19/32	1/ 8	1 3/ 8	3/ 4	3/ 4	1/ 8			**4 23/32**		-4.72
A503 -3 kV, 3 mA	6 3/ 8		5 1/ 2		3				**14 7/ 8**		-14.88
A503 +3 kV, 3mA				2 5/ 8					**2 5/ 8**		-2.63
A505 -3 kV, 200uA		5/16				1/ 4			**9/16**		-0.56
Positive low current									**0**		0.00
Low Voltage Supply											
Precision 0-10 V		1				1			**2**		-2.00
+- 5V 50 A		1				1			**2**		-2.00