Neutral Particle Spectrometer Data Acquisition Logic

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September 6, 2023

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1 Introduction

The Neutral Particle Spectrometer (NPS) consists of 1080 $PbWO_4$ crystals arranged in 30 columns and 36 rows. Each crystal is $2\times2\times20$ cm^3. Each crystal is readout by a Hamamatsu R4125 PMT coupled to a custom pre-amp. Each channel is connected (via $\sim$ 50 m of RG-58 coax) to the input of a JLab FADC250 module.

This note describes how the FADC250 and associated VTP and CAEN V1495 logic boards form the gamma-ray and π^0 triggers at the 250 MHz clock cycle. Trigger formation is controlled by the following global parameters defined in Table 1

Table 1: Global parameters for cluster and trigger formation in the NPS Calorimeter electronics.

Variable	Value	Units	Meaning
FADC parameters, stored in file /nps-vme/cfg/nps-vme1.cfg on host nps-vme			
hline FADC250_TET	10	MeV	Hit threshold
FADC250_NSB	4	Samples	# samples for integration Before hit
FADC250_NSA	9	Samples	# samples for integration After hit
FADC250_GAIN	1	MeV	MeV per FADC sample value. This value can be specific to each channel
VTP & V1495 parameters, stored in file nps-vtp:nps-vtp/cfg/nps-vtp.cfg			
Parameter prefix VTP_NPS_ECALCLUSTER			
_SEED_THR	50	MeV	Threshold for defining a cluster seed
_HIT_DT	20	ns	Coincidence window for cluster formation
_NHIT_MIN	1		Mininum # Hits to define cluster
_TRIGGER_THR	900	MeV	Single-cluster validation threshold (Bit 0)
_CLUSTER_PAIR_THR	500	MeV	Two-cluster validation threshold
_CLUSTER_PAIR_WIDTH	20	ns	Output width of VTP Bit 4
VTP_NPS_TRIG_WIDTH	20	ns	(Bit 0?) Output signal width: TS1
VTP_NPS_TRIG_LATENCY	3000	ns	Data buffer width
Hard-coded	20	ns	output width of VTP Bit 3: TS6
VTP Output Bits (each crate)			
VTP Bit 0	Cluster $\geq$ VTP_NPS_ECALCLUSTER_TRIGGER_THR		
VTP Bit 3	$\geq$ 1 cluster above ..._PAIR_THR in crate		
VTP Bit 4	$\geq$ 2 clusters > ..._PAIR_THR in crate		
Data Readout parameters			
FADC250_W_OFFSET	4500	ns	FADC Lookback time from trigger
FACD250_W_WIDTH	440	ns	Waveform readout window
VTP_W_OFFSET	4448	ns	VTP Lookback time time from trigger
VTP_W_WIDTH	1000	ns	Window width to find clusters
VTP_NPS_ECALCLUSTER _CLUSTER_READOUT_THR	100	MeV	Cluster threshold for readout
VTP_NPS_FADCMASK_MODE	1		0 for $5x5$, 1 for $7x7$ readout array

2 FADC250

Each channel of the 16-channel FADC250 module produces a 12-bit digitized value (0 to 4095) on a 0.0 to 1.0 volt scale every 4.0 nsec. The pedestal value is typically set to approximately 10% of full scale. Actual pedestal values have to be measured periodically, and uploaded to the module firmware.

A Hit is created in the clocked data stream of the FADC FPGA logic for every sample that is above (after pedestal subtraction) the threshold value FADC250_TET. The threshold is applied after multiplying the sample value by the gain (or conversion) factor FADC250_GAIN for that channel. The Hit value is a 13-bit word equal to the sum of the samples FADC250_NSB before and FADC250_NSB (inclusive of the Hit sample) after the first sample above threshold. Another Hit cannot be created until at least 8 samples after the Hit.

3 VTP

Each crate contains a VTP logic module that aggregates the data stream of Hit values from all FADC250 cards in the crate, as well as select channels from adjacent crates. Any Hit above the energy threshold VTP_NPS_ECALCLUSTER_SEED_THR is a candidate 'seed' for a cluster. A seed must also be a local maximum in space and time. For each seed, the VTP logic sums all Hits in the 3×3 array centered on the seed crystal. Hits in the 8 crystals surrounding the seed are included only if they occur within the time interval VTP_NPS_ECALCLUSTER_HIT_DT (a multiple of 4 ns) following the time of the seed Hit. Clusters are built around all seed Hits in real time. Thus it is possible that two clusters form that overlap both in crystal channels and within the time window ..._HIT_DT. If there is at least one Hit between the two seeds that is of lower amplitude than both seeds, then the two clusters retain their identities **but how are the Hit weights divided between clusters?**. If two seed Hits are not separated by a lower Hit, then the two clusters are merged into one and assigned to the larger seed Hit.

The stream of clusters is clocked through the VTP logic. Each cluster has a (14-bit?) energy value –saturated by *e.g.* FADC250_Gain$*(2^{14}-1)$– and remains in time relative to the seed Hit. Any cluster with an energy value in excess of
VTP_NPS_ECALCLUSTER_TRIGGER_THR
produces an output pulse on that VTP's output Bit 0 (of width VTP_NPS_TRIG_WIDTH).

When a VTP finds any cluster above energy threshold value VTP_NPS_ECALCLUSTER _PAIR_THR a pulse is asserted on output Bit 3. The width of this pulse is currently hard-coded, not a parameter, but it is intended to be the same value as VTP_NPS_ECALCLUSTER _CLUSTER_PAIR_WIDTH.

When a VTP finds at least two clusters, each above energy threshold value VTP_NPS _ECALCLUSTER_PAIR_THR within the time interval VTP_NPS_ECALCLUSTER_PAIR _WIDTH a pulse is asserted on output Bit 4.

4 V1495

The output bits from all five VTP modules from all five VME crates containing FADC250 modules are input to the single CAEN V1495 module.

The V1495 forms the logic OR of all Bit-0 signals and delivers this pulse stream to the TS1 NIM output sent via coax to the counting house over a cable of length XXX nsec.

In each clock cycle, the V1495 generates a true logic level (after delay) if the number of valid input Bit-3 signals was ≥ 2. This signal is then ORed with all of the input Bit-4 signals. The resulting output stream is delivered to the TS6 output, which is sent via coax to the counting house.

5 Readout

...more to come...

6 Commissioning

1. Take a random coincidence run (PS3 = 0, all others -1). Beam $5\,\mu$ A.
   - Check that most waveforms are at about sample#50 (200 ns).
   - Check in waveform analysis that VTP found all clusters.
2. Take a series of EDTM runs (PS1=0, others -1). Vary EDTM rate: 10, 100, 1000 Hz. Check event deadtime.